UDC 004.3

SELF-TIMED LOOK UP TABLE FOR ULAs AND FPGAs

Tyurin S. F. – Honored Inventor of the Russian Federation, Dr. Sc., Professor, Professor of the Automation and Telemechanic Department, "Perm National Research Polytechnic University", Perm, Russia.

Professor of the Software Computing Systems Department, "Perm State University", Perm, Russia.

Skornyakova A. Yu. – PhD, Design engineer of the JSC "Perm Scientific-Industrial Instrument Making Company", Perm, Russia.

Stepchenkov Y. A. – PhD, Head of the department, Institute of Informatics Problems, Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences, Moscow, Russia.

Diachenko Y. G. – PhD, Head of sector, Institute of Informatics Problems, Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences, Moscow, Russia.

ABSTRACT

Context. Self-Timed Circuits, proposed by D. Muller on the rise of the digital era, continues to excite researchers' minds. These circuits started with the task of improving performance by taking into account real delays. Then Self-Timed Circuits have moved into the field of green computing. At last, they are currently positioned mainly in the field of fault tolerance. There is much redundancy in Self-Timed Circuits. It is believed that Self-Timed Circuits approaches will be in demand in the nano-circuitry when a synchronous approach becomes impossible. Strictly Self-Timed Circuits check transition process completion for each gate's output. For this, they use so-called D. Muller elements (C-elements, hysteresis flip-flops, G-flip-flops). Usually, Self-Timed Circuits are designed on Uncommitted Logic Array. Now an extensive base of Uncommitted Logic Array Self-Timed gates exists. It is believed that Self-Timed Circuits are not compatible with FPGA technology. However, attempts to create self-timed FPGAs do not stop. The article proposes a Self-Timed Lookup Table for the Self-Timed Uncommitted Logic Array and the Self-Timed FPGA, carried out either by constants or utilizing additional memory cells. Authors proposed 1,2 – Self-Timed Lookup Table and described simulation results.

Objective. The work's goal is the analysis and design of the Strictly Self-Timed universal logic element based on Uncommitted Logic Array cells and pass-transistors circuits.

Methods. Analysis and synthesis of the Strictly Self-Timed circuits with Boolean algebra. Simulation of the proposed element in the CAD "ARC", TRANAL program, system NI Multisim by National Instruments Electronics Workbench Group, and layout design by Microwind. The reliability theory and reliability calculations in PTC Mathcad.

Results. Authors designed, analyzed, and proved the Self-Timed Lookup Table's workability for the Uncommitted Logic Arrays and FPGAs. Layouts of the novel logic gates are ready for manufacturing.

Conclusions. The conducted studies allow us to use proposed circuits in perspective digital devices.

KEYWORDS: Self-Timed, Lookup Table, Simulation.

ABBREVIATIONS

LUT is a Look up Table;
CDNF is a Canonic Disjunctive Normal Form;
DNF is a Disjunctive Normal Form;
ST is a Self-Timed;
STC is a Self-Timed Circuits;
SSTC is a Strictly Self-Timed Circuits;
FPGA is a Field-Programmable Gate Array;
IPI RAN is an Institute of Informatics Problems (Russia);
ULA is an Uncommitted Logic Array;
XOR is an exclusive OR.

NOMENCLATURE

F_1 is a logic function to realize;
F_2 is the dual logic function to realize;
i is the first math index;
j is the second math index;
k is the quantity of the conjunctions in DNF;
l is the number of circuit's levels;
n is the quantity of the input variables;
s_i is the configurable constant;
x is an input variable;
σ is the negation index.

INTRODUCTION

STC was proposed as a "fast" alternative to the synchronous computing paradigm, as a subspecies of asynchronous circuits [1]. In the USSR, until its liquidation, the STC topic was actively developed by Dr. Victor Varshavsky's research group [2]. The Varshavsky's group's members Dr. Marakhovsky V.B. in St. Petersburg Polytechnic University [3, 4], and Dr. S. Alex Yakovlev in the University of New Castle [5, 6], pick up the "STC banner". In Russian Federation, a research group from the Institute of Informatics Problems of the Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences investigates now STC problems [7, 8]. Automation and Telemechanic Department (Perm National Research Polytechnic University, Perm, Russia), Software Computing Systems Department (Perm State University, Perm, Russia) are science partners of the IPI RAN in STC direction since 1995. STC trend is active in world science [9–13]. We use such concepts as speed-independent circuits, semi-modular or/and distributive quasi-delay-insensitive circuits [7, 8]. As this area developed, it turned out that in some cases, the claimed increase in speed does not occur due to too large hardware costs increase. Therefore, we have aimed primary efforts at evaluating energy

DOI 10.15588/1607-3274-2021-1-4

efficiency in terms of gain in front of synchronous solutions. However, this direction became problematic after the development of synchronous Tri-Gate transistors [14]. Currently, STCs are positioned in the fault-tolerant solution segment. However, as we approach the molecular level of electronics and develop quantum computing, where quantum effects affect, it becomes clear that there is no alternative to STCs [15].

Nevertheless, this direction's development is constrained by the relatively high complexity of design based on ASIC or ULA. Synchronized FPGAs greatly simplify the design by configuring functions by so-called LUT [16, 18] and connections. In this regard, attempts to develop self-synchronous FPGAs do not stop [18–20]. However, configurable STC LUT gates are not thoroughly investigated. Therefore, a detailed review of constructing STC LUT, modeling, and evaluation is relevant.

The study object is the throughput strictly self-timed circuits, consisting of double combinational channels, indicators, and C-elements [4, 5].

The purposes of the work are to analyze and give a synthesis of the universal throughput strictly self-timed element for the ULAs and FPGAs.

1 PROBLEM STATEMENT

Given: Throughput or combinational, not universal STC. $F_1(x_1, x_2, ...x_n)$ is the logic function to realize. In a typical case, we have DNF $F_1(x_1, x_2, ...x_n) = \bigvee_{j=1}^{k} \&_{i=1}^{n_j} (x^{\sigma_i}{}_{i_j})$. $F_2(x_1, x_2, ...x_n)$ is a dual function, $F_2(x_1, x_2, ...x_n) = \&_{j=1}^{k} \vee_{i=1}^{n_j} (\bar{x}^{\sigma_i}{}_{i_j})$. There are 2NAND or 2 NOR indicators and C-elements [4, 5].

It is required: to design universal STC in CDNF, which is configured by special constants $s_i; i = 1, 2^n$:

$$F_1(x_1, x_2, ...x_n) = \bigvee_{j=1}^{2^n} \&_{i=1}^{n} (s_i x^{\sigma_i}{}_i);$$

$$F_2(x_1, x_2, ...x_n) = \bigvee_{j=1}^{2^n} \&_{i=1}^{n} (\bar{s}_i x^{\sigma_i}{}_i).$$

It is needed to design a new element's architecture based on ULA and LUT FPGA logic elements and perform functional and layout simulations in NI Multisim by National Instruments Electronics Workbench Group and layout design by Microwind of the proposed element. An additional important task is a semi-modularity check by special software TRANAL. It is necessary to estimate new technical decision by reliability methods and perform calculations in PTC Mathcad.

2 REVIEW OF THE LITERATURE

Fig. 1 shows the current traditional synchronous throughput logic [13] in the so-called Register Transfer Level (RTL). Due to Input-Output Latches (RGs), we can parry the negative transition processes (glitches).

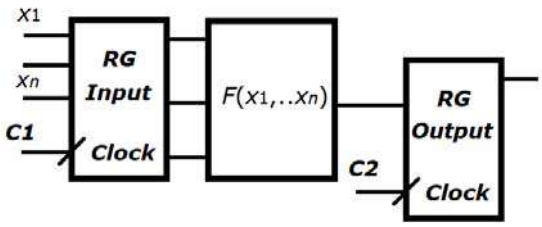


Figure 1 – Traditional synchronous throughput logic

First clock impulse C1 fixes an input vector. Then the logic function is calculated after that second clock impulse C2 is coming. Therefore, the frequency must accord to the worst case, significantly reducing the circuits' speed, unfortunately. Asynchronous circuits work according to real delays but require complicated design procedures to find all transition processes' hazards. One kind of asynchronous circuit is the so-called STC. It uses a request-and-acknowledge handshake protocol [7, 8, 10, 13]. The block AND (Fig. 2) receives a dual-rail input vector from previous gates only by request from C-element fixing (2NOR+NOT) indicator's transition termination and C-element's transition completion.

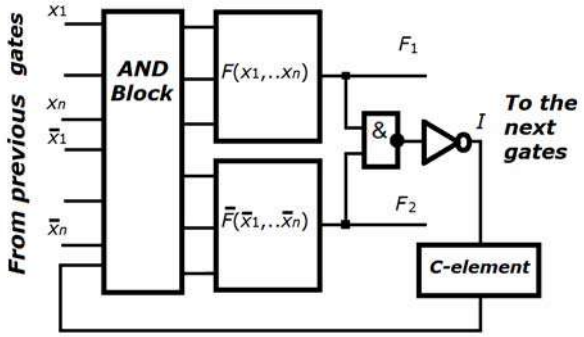


Figure 2 – ST throughput logic

In the working phase, $F_1 = \overline{F}_2$ due to I=0; in the so-called spacer phase, $F_1 = F_2$, for example, $F_1 = F_2 = 1$ and I=1. Therefore, we have such sequence: initial state, the C-element's output = 0, this is a spacer, then I=1 and C-element is set in 1. Then the unit receives the first dual-rail input vector, I=0 and C-element is set to 0 after calculation. Then process repeats.

C-element forms a signal acknowledging the input vector's readiness of the next gates. So in a typical case, block AND must receive an enable signal from the last C-element when calculations end in all strings of gates.

SST (semi-modularity circuits) throughput logic indicates all inputs too (Fig. 3). Each pair of the dual-rail outputs of the AND block needs an indicator, which activates an additional C-element. Main C-element receives the input transition completion signal and forms the total completion signal for input and output transitions. If the transition process does not complete, for example, due to failures, the main C-element does not

DOI 10.15588/1607-3274-2021-1-4

generate such a signal, increasing digital circuits' reliability.

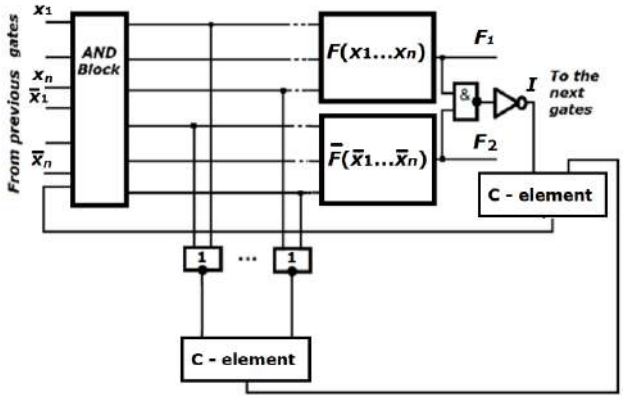


Figure 3 – SST throughput logic

Paper [13] proves STC's effectiveness in the viewpoint of speed and energy dissipation. Article [19], according to the authors, considers a hazard-free self-timed LUT. They talk about asynchronous FPGA. However, this is not correct.

The same discrepancy exists in [18], describing the handshake protocol of FPGA Speedster22i (Achronix). Paper [20] proposes ST Delay Sensor for Field FPGAs. It describes the sensor, which is just asynchronous, and the logical function calculations are not asynchronous. We have not found universal SST logic elements (LUTs) in the available sources [1–20].

3 MATERIALS AND METHODS

Universal implementation of a self-timed unit calculating logical functions is possible based on so-called LUT.

LUT [15–17] for n variable or 2^n function generator is n–to–1 multiplexor. It is easy to see that the dual multiplexer is implemented using dual settings. Elementary dual-channel generator, or single variable x 2–to–1 multiplexor, configurable by s constants, is described by expressions (1):

$$\begin{cases} F_1(s_0 s_1 x) = s_0 \bar{x} \vee s_1 x; \\ F_2(s_0 s_1 x) = \bar{s}_0 \bar{x} \vee \bar{s}_1 x. \end{cases} \quad (1)$$

Indeed accordingly to Boolean algebra (common gluing law), we have :

$$\overline{F}_1(s_0 s_1 x) = \overline{s_0 \bar{x} \vee s_1 x} = (\bar{s}_0 \vee x)(\bar{s}_1 \vee \bar{x}) = \bar{s}_0 \bar{s}_1 \vee \bar{s}_0 \bar{x} \vee \bar{s}_1 x = \bar{s}_0 \bar{x} \vee \bar{s}_1 x. \quad (2)$$

Fig.4. shows single variable LUT with dual channels based on 2AND-2OR-NOT gate. One NOT gate provides $\bar{x}$ variable, next two NOT gates provide $\bar{s}_0, \bar{s}_1$ for the dual channels (Fig. 4). Table 1 shows the truth table of the 1-LUT with dual channels.

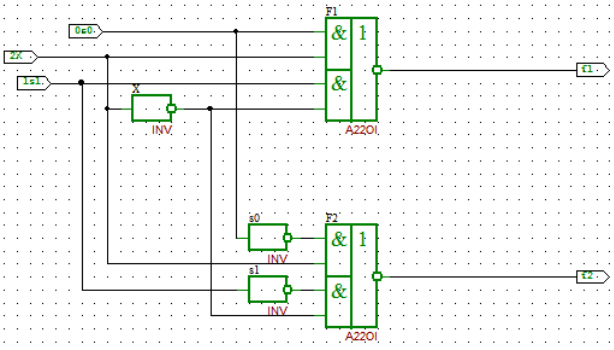


Figure 4 – Single variable 1-LUT with dual channels

Table 1 – Table of the1-LUT with dual-channel simulation

№	S0	S1	X	F1	F2
1	0	0	0	1	0
	0	0	1	1	0
2	1	0	0	1	0
	1	0	1	0	1
3	0	1	0	0	1
	0	1	1	1	0
4	1	1	0	0	1
	1	1	1	0	1

Table 1 confirms the realization of any single variable logic function. Dual outputs allow checking unit operation. Using three 2AND-2OR-NOT gates, we get 2-LUT with dual channels, presented in Fig. 6.

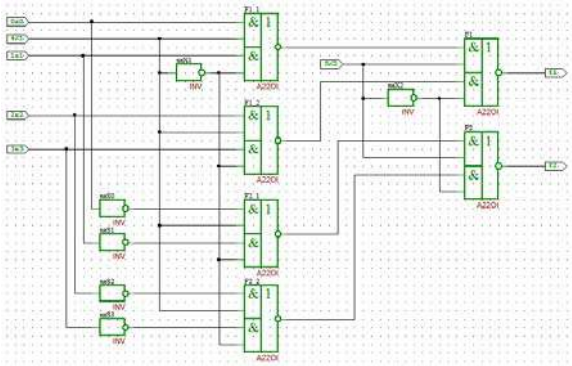


Figure 5 – 2-LUT with dual channels (two levels)

Fig. 5 confirms that new 2AND-2OR-NOT gate-level i provides inversion of the transmitted constant. If a number of levels is an even (l=n), constants s inversion is not required to get on F1 the same s; $\sigma = 0$. If the number is an odd, it is required. $\sigma = 1, \bar{s}$ according to expression (3).

$$s^{\sigma}; \sigma = 1 if [(2i-1) = n] = true; \quad \sigma = 0 if [2i = n] = true. \quad (3)$$

DOI 10.15588/1607-3274-2021-1-4

The “indication” is the most critical STC procedure. For the SST LUT design, based on Figs. 4, 5, it is required to indicate input variables *x* and 2AND-2OR-NOT gates’ outputs. The configurable constant is not indicated. Therefore, SST LUT design needs special gates and D. Muller C-elements [7, 8]. Dual-rail variables are also used. We use Russian CAD “ARC,” USA system NI Multisim by National Instruments Electronics Workbench Group and layout design by Microwind, the foundation of reliability theory and reliability calculations in PTC Mathcad. For the semi-modularity checking, TRANAL program of the IPI RAN is used [7].

4 EXPERIMENTS

Let us propose ST-LUT for the 2AND-2OR-NOT base (for ULA) and based on traditional pass transistor LUT (for FPGA) accordingly to Fig. 3. Figs. 4, 5 show proposed ULA implementation based on 2AND-2OR-NOT LUT with dual channels. Using additional C-elements (hysteretic triggers, H-triggers) and indicators 2NAND+NOT, we get Fig. 6 after the experiment.

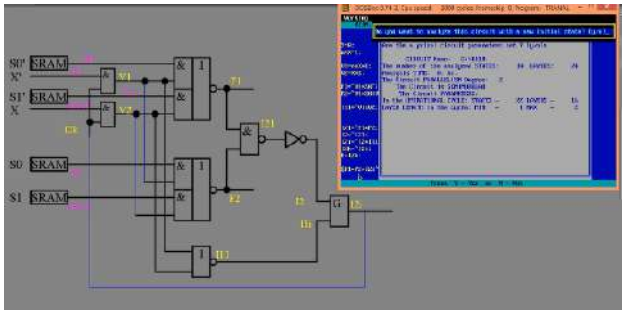


Figure 6 – 1-LUT2AND-2OR-NOT based, successful semi-modular checking experiment in TRANAL program

So semi-modular of the 1-LUT2AND-2OR-NOT based is proved. The task is to consider and design 2-LUT2AND-2OR-NOT based and propose standard rules of construction n-LUT2AND-2OR-NOT for ULA. Next, let us try to implement 1-LUT-ST based on pass transistors (FPGA technology) [15, 17]. Early, authors proposed 1-LUT-ST based on pass transistors using p-MOS pass transistors for the spacer sub circuit (Fig. 7).

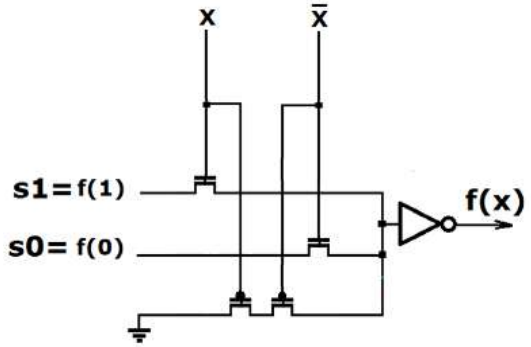


Figure 7 – First variant of the 1-LUT-ST based on pass transistors using p-MOS spacer sub circuit (single channel)

Static logic simulation in Multisim [21] was correct, but dynamic layout simulation in Microwind [22] demonstrated “bad” waveforms (Fig. 8).

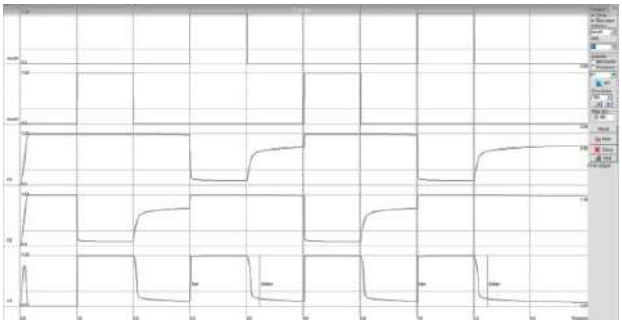


Figure 8 – XOR realization waveform diagrams of the first variant 1-LUT-ST layout simulation

It was decided to unify the transistors and introduce a spacer chain of n-MOS transistors. Fig. 9 shows a new design. Fig. 10 shows a new 1-LUT-ST layout simulation and confirms the decision correctness. However, it may seem that such an option (Fig. 10a) is not better than the option shown in Fig. 4 (2AND-2OR-NOT gate). Indeed, we have ten transistors (Fig. 9a) versus eight (Fig. 10).

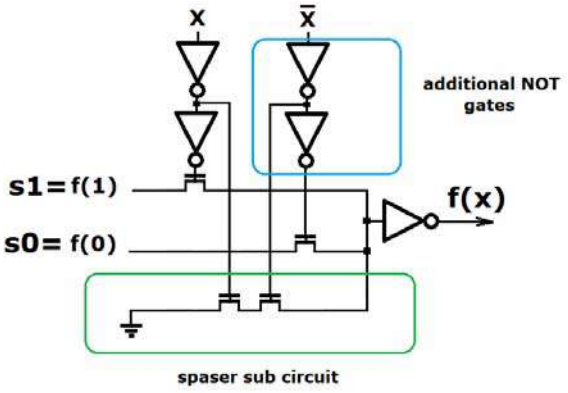
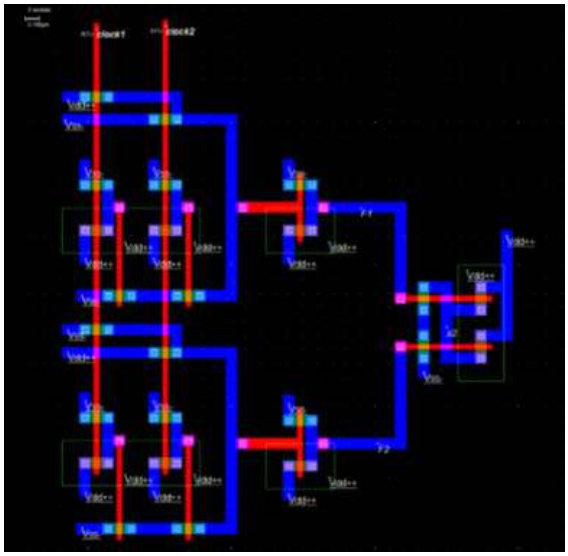


Figure 9 – New pass transistor circuit for 1-LUT-ST (single channel)

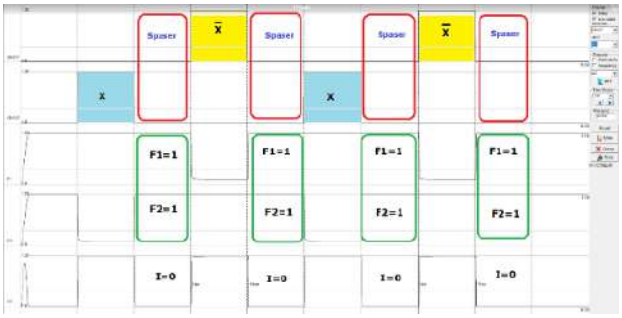
However, the performance decreases compared to Fig. 6 slightly: the maximum delay increases by the one transistor delay in the output NOT gate.

We did a triple simulation of proposed novel logic elements in the CAD “ARC,” TRANAL program, system NI Multisim by National Instruments Electronics Workbench Group, and layout design by Microwind. Using the described experiments, we got the following new results.

DOI 10.15588/1607-3274-2021-1-4



a



b

Figure 10 – New 1-LUT-ST simulation for the XOR function: a – new 1-LUT-ST layout; b – "good" waveforms of the new 1-LUT-ST, marking operational and spacer phases

5 RESULTS

We perform functional simulation in CAD "Multisim." Fig. 11 shows the proposed 1-LUT-ST pass transistor simulation in CAD "Multisim." The main circuit consists of transistors Q1 (not X) and Q2 (X) (Fig. 11a). Spacer circuit consists of transistors Q3 and Q4. In the not (X=X=0) case, the spacer circuit transmits zero level to the output of the 1-LUT-ST (Fig. 11a).

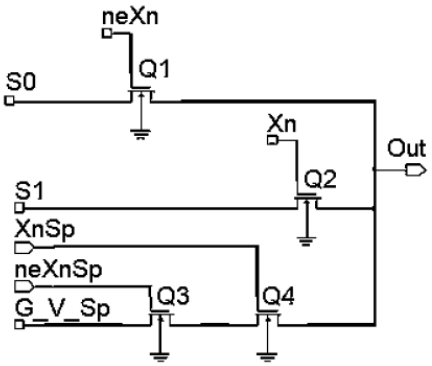
Fig. 11b presents the XOR(X1, X2) waveform of the 2-LUT-ST.

In the study, the authors set the features of alternating types of indicators for 2-LUT (ULA) relatively 1-LUT (Fig. 12 a). The type of spacer on the next layer changes; accordingly, the types of indicators also change. Besides, the block for receiving variables also changes. If the first layer contains AND cells, then the second one contains OR cells. Here such regularity was found: in the first layer, the indicators of inputs are 2NOR cells and output AND cells; in the second layer, on the contrary, input indicators AND cells, and output 2NOR cells.

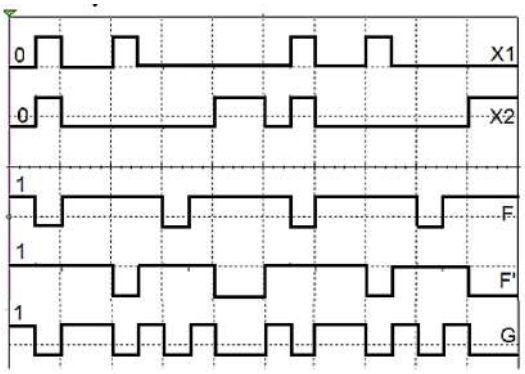
A TRANAL program was used (Fig. 12b) to evaluate semi-modularity, the results of which confirm strict self-timing of proposed circuit (Fig. 12c).

Fig. 12d shows successful results of the 1-LUT-ST pass transistor TRANAL simulation.

The TRANAL simulation of the 2-LUT-ST was successful, too (Fig. 12 e).



a



b

Figure 11 – "Multisim" simulation: a) 1-LUT-ST; b) XOR waveform of the 2-LUT-ST

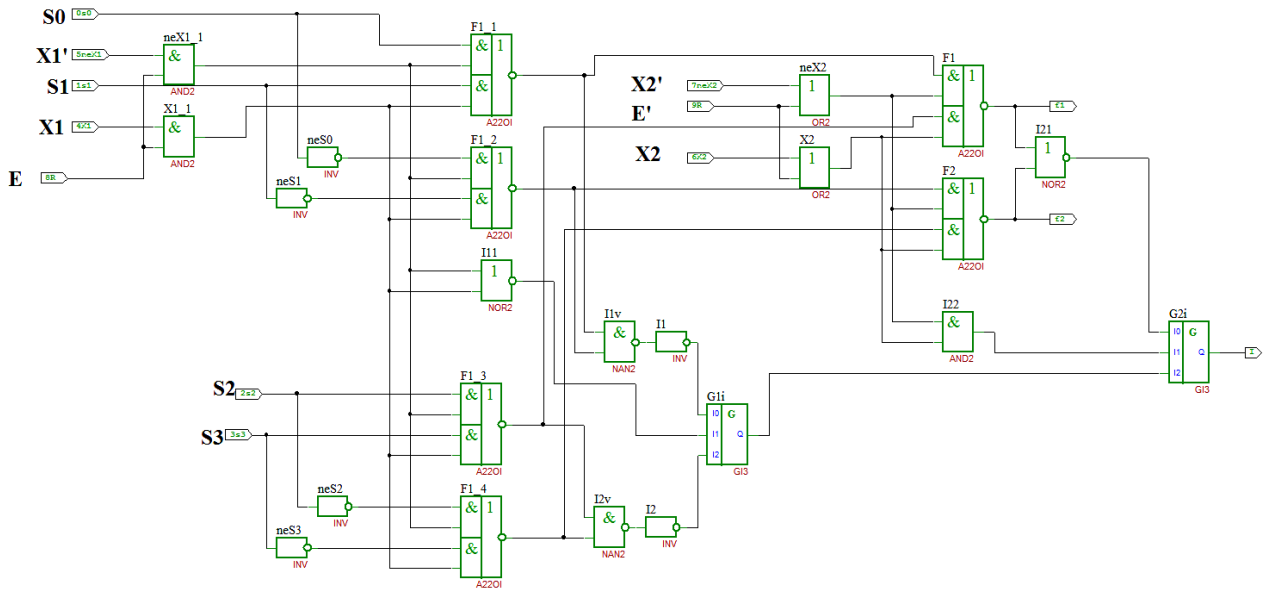
Fig. 12 f shows the proposed layout. Fig. 12g demonstrates the waveform of the 1-LUT-ST.

Fig. 12h shows the XOR waveform of the 2-LUT-ST. Table 2 shows comparisons of the LUT-ST-ULA and LUT-ST pass transistor (p.t.) by power consumption P (μW), area S (μm^2), delay T (ps) and number of transistors N (pieces).

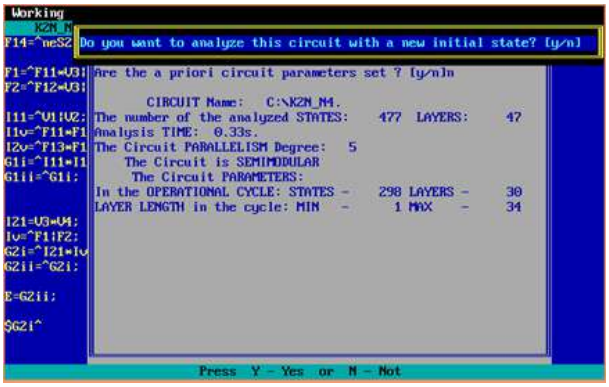
Table 2 – Comparison by area S, power consumption P, delay T and number of transistors N

Gate	Number of arguments		
	n=1	n=2	n=3
LUT-ST-ULA	P =159,7 μW	P =418,8 μW	P =930,2 μW
	S =159,7 μm^2	S =418,8 μm^2	S =930,2 μm^2
	T= 34 ps	T= 35 ps	T= 40 ps
	N= 46 pcs	N=139 pcs	N=355 pcs
LUT-ST p. t.	P =35,64 μW	P =100 μW	P =207 μW
	S =123,7 μm^2	S =402,4 μm^2	S =1092 μm^2
	T= 52 ps	T= 99 ps	T= 154 ps
	N=61 pcs	N=149 pcs	N=362 pcs

DOI 10.15588/1607-3274-2021-1-4



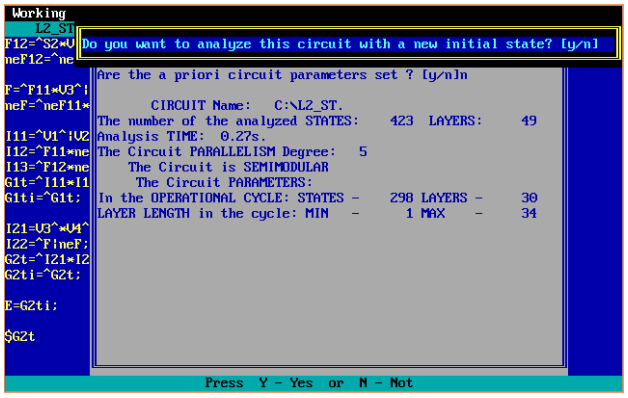
a



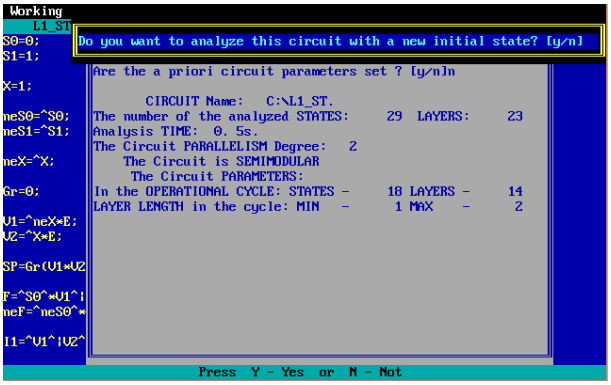
b

S0=1; S1=0; neS0=0; neS1=1; X=1; neX=0;	Constants
V1=X*E; V2=neX*E; V3=X*E; V4=neX*E;	Inputs of the main and dual channels
F1=^S0*V1|S1*V2;	Main channel description
F2=^neS0*V3|neS1*V4;	Dual channel description
I11=^V1|V2; I12=^V3|V4;	Inputs indicators
I1i=^I11*I12|I1(I11|I12); I1=^I1i;	C-element 1
I21=^F1*F2; I2=^I21;	Outputs indicators
I2i=^I2*I1|I2k(I2|I1); I2k=^I2i;	C-element 2
E=I2k;	Control signal
SF1*F2*I2i ^	Initials states

c

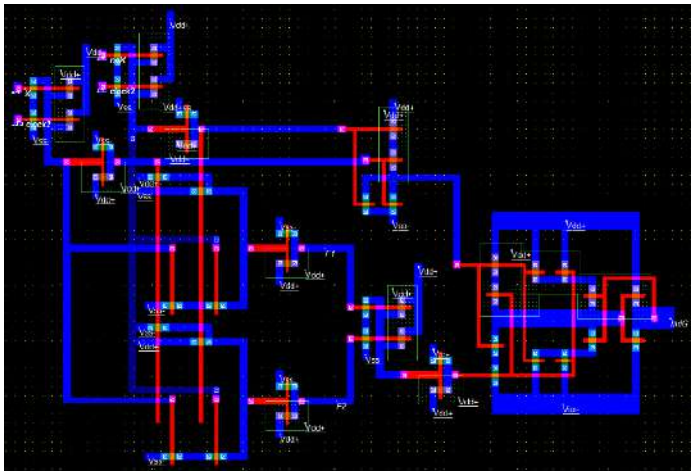


d

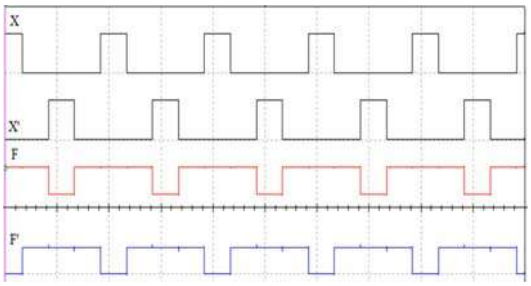


e

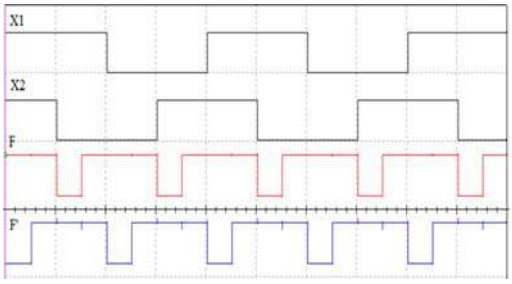
DOI 10.15588/1607-3274-2021-1-4



f



g



h

Figure 12 – Results of the proposed gates simulation: a – 2-LUT-ST-ULA model in "ARC" CAD; b – TRANAL-program; c – successful results of the 2-LUT-ST-ULA TRANAL simulation; d – successful results of the 1-LUT-ST pass transistor TRANAL simulation; e – successful results of the 2-LUT-ST pass transistor TRANAL simulation; f – 1-LUT-ST layout; g – waveform of the 1-LUT-ST (s0=0, s1=1) ; h – XOR waveform of the 2-LUT-ST (s0=0, s1=1,s2=1, s3=0)

Comparison shows that LUT-ST-ULA is preferable to LUT-ST p.t. in terms of power consumption. This is because LUT-ST-ULA uses CMOS technology to implement a multiplex tree. Nevertheless, implementation 2 is preferable from the point of view of work under conditions of exposure to charged particles, since the configuration is set "rigidly".

6 DISCUSSION

Investigation of the proposed LUT-ST in Fig. 12, 13 allows for calculating its reliability. The failure-free operation probability (λ – is single transistors failure rate, t – is time, α – is the Weibull distribution coefficient) of the entire circuit is shown by expression (4).

$$P(t) = e^{-(46)\cdot\lambda\cdot t^{\alpha}}. \quad (4)$$

Taking into account duplication, we can get expression (5).

$$P_{1-LUT-ST^*} = [e^{-(12)\times\lambda\cdot t^{\alpha}} + 2e^{-(6)\cdot\lambda\cdot t^{\alpha}}(1-e^{-(6)\cdot\lambda\cdot t^{\alpha}})]e^{-(34)\cdot\lambda\cdot t^{\alpha}}. \quad (5)$$

Using transistors quadding [22, 23] only for the H-trigger we can get expression (6) and curves, displayed in Fig. 14.

$$P_{1-LUT-STQ} = [e^{-(12)\cdot\lambda\cdot t^{\alpha}} + 2e^{-(6)\times\lambda\cdot t^{\alpha}}(1-e^{-(6)\cdot\lambda\cdot t^{\alpha}})]e^{-(22)\cdot\lambda\cdot t^{\alpha}} \cdot \cdot[e^{-(4\cdot12)\cdot\lambda\times t^{\alpha}} + 2e^{-(3\cdot12)\cdot\lambda\cdot t^{\alpha}}(1-e^{-(12)\cdot\lambda\cdot t^{\alpha}})]. \quad (6)$$

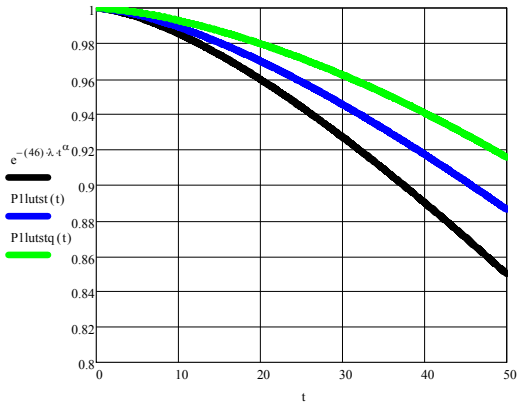


Figure 14 – Channel duplication reliability $P_{1LUTST}(t)$ in comparison with $P_{1-LUTSTQ}(t)$ and $e^{-(46)\cdot\lambda\cdot t^{\alpha}}$; $\lambda = 10^{-5}, \alpha = 1,5$.

This way much improves reliability. Thus, Fig. 13 proves that the probability of uptime is increased by about 20% of the maximum possible gain (up to 1). However, in the authors' opinion, due to considerable redundancy of quadding and fundamental Mead-Conway restrictions [24], the sliding backup option is more perspective. However, this requires buffers with three states, and consideration of such issues is expected in further studies.

DOI 10.15588/1607-3274-2021-1-4

CONCLUSIONS

Therefore, we propose advanced LUT by adding two NOT gates and an additional tree branch for the ST throughput logic realization. We found that such an implementation is preferable in the number of transistors than the 2AND-2OR-NOT implementation. We developed the layout of the proposed unit. We performed a corresponding simulation, which confirmed the performance of the proposed LUT-ST with a hysteretic trigger. The developed LUT improves FPGA's reliability by monitoring the transition's completion, and no clock generator is required. Besides, the developed LUT provides ultra-low voltage operation. Such approaches are supposed to ensure the operation of nano-electronic structures under conditions of quantum uncertainty.

The scientific novelty of obtained results is that the proposed universal gates open a new STC subclass.

The practical significance of the obtained results lies in the fact that the proposed gates' functional and layout simulation confirms their effectiveness. Furthermore, the proposed gates create the base for advanced self-timed FPGAs.

Prospects for further research are to study the problem of checking out and diagnosing proposed universal self-timed gates. Also, it is advisable to develop LUT for a larger number of variables (3, 4, 5, 6, 7).

ACKNOWLEDGEMENTS

This research was carried out with the support of the Department of Automation and Remote Control of the Perm National Research Polytechnic University (Head of the department Prof. Yuzhakov Alexander Anatolievich) and the Department of Software Computing Systems of the Perm State University.

Great thanks to the PhDs Ruslan Vikhorev (Perm scientific-industrial instrument making company) and Irina A. Barinova (Perm National Research Polytechnic University).

This work was supported in part by a grant from EU by TEMPUS-GreenCo (530270-TEMPUS-1-2012-1-UK-TEMPUS-JPCR) with the assistance of the Department "Computer Systems and Networks" Kharkiv National Aerospace University named after V. E. Zhukovsky "HAI". The research was funded by a grant from the Russian Science Foundation (Project № 19-11-00334).

REFERENCES

1. Muller D. E., Bartky W. S. A theory of asynchronous circuits, *On the Theory of Switching, Part 1*. Harvard, University Press, 1959, pp. 204–243.
2. Varshavsky V. I. Ed. Aperiodic Automata. Moscow, Nauka, 1976, 304p.
3. Marakhovsky V. B., Surkov A. V. Globally asynchronous system of interactive Moore state machines, *IET Computers and Digital Techniques*, 2016, Vol. 10, Issue 4, pp. 186–192.
4. eds.: Cortadella Jordi, Yakovlev Alex and Rozenberg Grzegorz GALA (Globally Asynchronous – Locally Arbitrary) Design'', LNCS 2549, Concurrency and Hardware Design, Advances in Petri Nets. Berlin, Springer, 2002, pp. 61–107.
5. Yakovlev A. Energy-modulated computing, *In Design, Automation & Test in Europe Conference & Exhibition (DATE), IEEE*, 2011, pp. 1–6.
6. Sokolov Danil, Khomenko Victor, Mokhov Andrey et al Automating the Design of Asynchronous Logic Control for AMS Electronics, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2020, Volume 39, Issue 5, pp. 952–965. DOI: 10.1109/TCAD.2019.2907905
7. Stepchenkov Y. A., Zakharov V. N., Rogdestvenski Y. V. et al. Speed-independent floating point coproceccor / [] // *IEEE East-West Design & Test Symposium: International, 26–29 Sept. 2015:proceedings.* Batumi, Georgia, IEEE, 2015, pp. 7493110. DOI: 10.1109/EWDTS.2015.7493110
8. Smith S. C. Design of an FPGA Logic Element for Implementing Asynchronous NULL Convention Logic Circuits [Electronic resource], Available at: https://ieeexplore.ieee.org/document/4231891 DOI: 10.1109/TVLSI.2007.898726
9. Self-timed Circuits [Electronic resource]. Access mode: https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-004-computation-structures-spring-2017/c7/c7s2/c7s2v5/self-timed-circuits-6-21-/
10. Walker A., Lala K. An Approach for Self-Timed Synchronous CMOS Circuit Design [Electronic resource], Access mode: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20040068174.pdf
11. Nielsen L. S., Niessen C., Sparsø J., Berkel van. C. H. Low-power operation using self-timed circuits and adaptive scaling of the supply voltage [Electronic resource], Access mode: https://backend.orbit.dtu.dk/ws/files/4151035/Nielsen.pdf
12. Masashi I., Takashi N. Performance Comparison between Self-timed Circuits and Synchronous Circuits Based on the Technology Roadmap of Semiconductors [Electronic resource], Access mode: http://webhost.laas.fr/TSF/WDSN08/2ndWDSN08(LAAS)_files/Texts/WDSN08-05-Imai.pdf
13. Kenny R., Watt J. The Breakthrough Advantage for FPGAs with Tri-Gate Technology [Electronic resource]. Access mode:URL:https://www.altera.com/en_US/pdfs/literature/wp/wp-01201-fpga-tri-gate-technology.pdf
14. Tyurin S. F. LUT based Fredkin gate, *Radio Electronics, Computer Science, Control*, 2020, No. 1, pp. 44–53.
15. Drozd A. V., Drozd M., Martynyuk O., Kuznietsov M. Improving of a Circuit Checkability and Trustworthiness of Data Processing Results in LUT-based FPGA Components of Safety-Related Systems, *CEUR Workshop Proceedings*, 2017, Vol. 1844, pp. 654–661.
16. Drozd A.V., Drozd M., Kuznietsov M. Use of Natural LUT Redundancy to Improve Trustworthiness of FPGA Design, *CEUR Workshop Proceedings*, 2016, Vol. 1614, pp. 322–331.
17. Speedster22i Configuration User Guide [Electronic resource]. – Access mode: http://www.achronix.com/wp-content/uploads/docs/Speedster22i_Configuration_User_Guide_UG033.pdf
18. Maheswaran K., Akella V. Hazard-free implementation of the self-timed cell set in a Xilinx FPGA [Electronic resource]. Access mode: http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.39.4276&rep=rep1&type=pdf
19. Osuna C. G., Ituero P. and López-Vallejo M. A Self-Timed Multipurpose Delay Sensor for Field Programmable Gate Arrays (FPGAs) [Electronic resource]. Access mode: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC3926550/
20. National Instruments [Electronic resource]. Access mode: http://www.ni.com/multisim/
21. Microwind & Dsch Version 3.5 [Electronic resource]. Access mode: http://auto.teipir.gr/sites/default/files/microwind_manual_lite_v35.pdf

DOI 10.15588/1607-3274-2021-1-4

22. Tyurin S. F. Investigation of a Hybrid Redundancy in the Fault-Tolerant Systems, *Radio Electronics, Computer Science, Control*, 2019, No. 2, pp. 23–33. DOI: 10.15588/1607-3274-2019-2-3
23. El-Maleh A. H., Al-Yamani A., Al-Hashimi B. M. Transistor-Level Defect Tolerant Digital System Design at the Nanoscale. Research Proposal Submitted to Internal Track Research Grant Programs [Electronic resource]. Access mode: http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.474.3844&rep=rep1&type=pdf
24. Mead C. A., Conway L. Introduction to VLSI Systems [Electronic resource]. Access mode: https://www.researchgate.net/publication/234388249_Introduction_to_VLSI_systems

Received 27.10.2020.
Accepted 27.01.2021.

УДК 004.93

САМОСІНХРОННИЙ ГЕНЕРАТОР ФУНКЦІЙ ДЛЯ БМК И ПЛІС

Тюрін С. Ф. – Заслужений винахідник Російської Федерації, д-р техн. наук, професор, професор кафедри автоматики і телемеханіки Пермського національного дослідницького політехнічного університету, Пермь, Росія.

професор кафедри математичного забезпечення обчислювальних систем Пермського державного національного дослідницького університету, Пермь, Росія.

Скорнякова А. Ю. – канд. техн. наук, інженер-конструктор Пермської науково-промислової приладобудівної компанії, Пермь, Росія.

Степченков Ю. А. – канд. техн. наук, начальник відділу інституту проблем інформатики, Російська академія наук, Москва, Росія.

Дьяченко Ю. Г. – канд. техн. наук, начальник сектора інституту проблем інформатики, Російська академія наук, Москва, Росія.

АНОТАЦІЯ

Актуальність. Самосинхронні схеми, запропоновані Д. Маллером на зорі цифрової ери, продовжують хвилювати уми дослідників. Ці схеми стартували із завдань підвищення продуктивності з урахуванням реальних затримок. Потім самосинхронні схеми перейшли в область «зелених» обчислень і, нарешті, в даний час позиціонуються в основному в області відмовостійкості. У самосинхронних схем багато надмірності. Вважається, що підходи самосинхронних схем будуть задіяні в нано схемотехниці, коли синхронний підхід стане неможливим. Строго самосинхронні схеми аналізують закінчення перехідного процесу на виходах кожного вентиля, використовуючи так звані елементи Маллера (С-елементи, гістерезисні тригери, G-тригери). Зазвичай самосінхронні схеми розробляються для базових матричних кристалів. Є велика база самосинхронних схем базових матричних кристалів. Вважається, що самосинхронні схеми несумісні з технологією FPGA. Але спроби створення самосинхронних ПЛІС не припиняються. У статті пропонується самосинхронний генератор функцій для самосинхронних схем базових матричних кристалів та самосинхронних FPGA, конфігурація яких здійснюється або константами, або за допомогою додаткових елементів пам'яті. Автори запропонували 1,2 – LUT-самосинхронний і описали результати моделювання.

Мета. Метою даної роботи є аналіз і проектування самосинхронного універсального логічного елемента LUT-самосинхронний, заснованого на елементах БМК і на схемах передачі транзисторів.

Методи. Аналіз і синтез строго самосинхронних схем за допомогою булевої алгебри. Моделювання запропонованого елемента в САПР «Ковчег», програмою TRANAL, системах NI Multisim від National Instruments Electronics Workbench Group і топологічного проектування Microwind. Теорія надійності і відповідні розрахунки в СКА Mathcad.

Результати. Автори розробили, проаналізували і довели працездатність самосинхронного генератора функцій для базових матричних кристалів і для ПЛІС. Топології нових логічних елементів готові до виготовлення.

Висновки. Проведені дослідження дозволяють використовувати запропоновані схеми в перспективних цифрових пристроях.

КЛЮЧОВІ СЛОВА: самосинхронний, генератор функцій, моделювання.

УДК 004.93

САМОСИНХРОННЫЙ ГЕНЕРАТОР ФУНКЦИЙ ДЛЯ БМК И ПЛИС

Тюрин С. Ф. – Заслуженный изобретатель Российской Федерации, д-р техн. наук, профессор, профессор кафедры автоматики и телемеханики Пермского национального исследовательского политехнического университета, Пермь, Россия.

профессор кафедры математического обеспечения вычислительных систем Пермского государственного национального исследовательского университета, Пермь, Россия.

Скорнякова А. Ю. – канд. техн. наук, инженер-конструктор, ПАО «Пермская научно-производственная приборостроительная компания», Пермь, Россия.

Степченков Ю. А. – канд. техн. наук, начальник отдела института проблем информатики, Российская академия наук, Москва, Россия.

Дьяченко Ю. Г. – канд. техн. наук, начальник сектора института проблем информатики, Российская академия наук, Москва, Россия.

АННОТАЦИЯ

Актуальность. Самосинхронные схемы, предложенные Д. Маллером на заре цифровой эры, продолжают волновать умы исследователей. Эти схемы стартовали с задач повышения производительности с учетом реальных задержек. Затем самосинхронные схемы перешли в область «зеленых» вычислений и, наконец, в настоящее время позиционируются в основном в области отказоустойчивости. В самосинхронных схемах много избыточности. Считается, что подходы самосинхронных схем будут востребованы в нано-схемотехнике, когда синхронный подход становится невозможным. Строго самосинхронные схемы анализируют окончание переходного процесса на выходах каждого вентиля, используя так называемые элементы Маллера (С-элементы, гистерезисные триггеры, G-триггеры). Обычно самосинхронные схемы разрабатываются для базовых матричных кристаллов. Имеется обширная база самосинхронных схем базовых матричных

DOI 10.15588/1607-3274-2021-1-4

кристаллов. Считается, что самосинхронные схемы несовместимы с технологией FPGA. Но попытки создания самосинхронных ПЛИС не прекращаются. В статье предлагается строго самосинхронный генератор функций для самосинхронных схем базовых матричных кристаллов и самосинхронных FPGA, конфигурирование которых осуществляется либо константами, либо с помощью дополнительных ячеек памяти. Авторы предложили 1,2 – LUT-самосинхронный и описали результаты моделирования.

Цель. Целью данной работы является анализ и проектирование строго самосинхронного универсального логического элемента LUT, основанного на элементах БМК и на схемах из передающих транзисторов.

Методы. Анализ и синтез строго самосинхронных схем с помощью булевой алгебры. Моделирование предложенного элемента в САПР «Ковчег», программе TRANAL, системах NI Multisim от National Instruments Electronics Workbench Group и топологического проектирования Microwind. Теория надежности и соответствующие расчеты в СКА Mathcad.

Результаты. Авторы разработали, проанализировали и доказали работоспособность самосинхронных генераторов функций для базовых матричных кристаллов и для ПЛИС. Топологии новых логических элементов готовы к изготовлению.

Выводы. Проведенные исследования позволяют использовать предложенные схемы в перспективных цифровых устройствах.

КЛЮЧЕВЫЕ СЛОВА: самосинхронный, генератор функций, моделирование.

ЛІТЕРАТУРА / ЛИТЕРАТУРА

1. Muller D. E. A theory of asynchronous circuits / D. E. Muller, W. S. Bartky // On the Theory of Switching, Part 1. – Harvard: University Press, 1959. – P. 204–243.
2. Aperiodic Automata / [Ed. V.I. Varshavsky] – M. : Nauka, 1976. – 304 p.
3. Marakhovsky V. B. Globally asynchronous system of interactive Moore state machines // V. B. Marakhovsky, A. V. Surkov // IET Computers and Digital Techniques. – 2016. – Vol. 10, Issue 4. – P. 186–192.
4. GALA (Globally Asynchronous – Locally Arbitrary) Design'', LNCS 2549, Concurrency and Hardware Design, Advances in Petri Nets / [eds.: Jordi Cortadella, Alex Yakovlev, and Grzegorz Rozenberg]. – Berlin : Springer, 2002. – P. 61–107.
5. Yakovlev A. Energy-modulated computing. In Design, Automation & Test in Europe Conference & Exhibition (DATE) / A. Yakovlev. – IEEE, 2011. – P. 1–6.
6. Automating the Design of Asynchronous Logic Control for AMS Electronics / [Danil Sokolov, Victor Khomenko, Andrey Mokhov, et al.] // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. – 2020. – Vol. 39, Issue 5. – P. 952–965. DOI: 10.1109/TCAD.2019.2907905
7. Speed-independent floating point coprocеccor / [Y. A. Stepchenkov, V. N. Zakharov, Y. V. Rogdestvenski, et al.] // IEEE East-West Design & Test Symposium: International, 26–29 Sept. 2015: proceedings. – Batumi, Georgia : IEEE, 2015. – P. 7493110. DOI: 10.1109/EWDTS.2015.7493110
8. Smith S. C. Design of an FPGA Logic Element for Implementing Asynchronous NULL Convention Logic Circuits [Electronic resource] / S. C. Smith. – Available at: https://ieeexplore.ieee.org/document/4231891 DOI: 10.1109/TVLSI.2007.898726
9. Self-timed Circuits [Electronic resource]. – Access mode: https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-004-computation-structures-spring-2017/c7/c7s2/c7s2v5/self-timed-circuits-6-21-/
10. Walker A. An Approach for Self-Timed Synchronous CMOS Circuit Design [Electronic resource] / A. Walker, P. K. Lala. – Access mode: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20040068174.pdf
11. Nielsen L. S. Low-power operation using self-timed circuits and adaptive scaling of the supply voltage [Electronic resource] / L. S. Nielsen, C. Niessen, J. Sparsø, C. H. van. Berkel. – Access mode: https://backend.orbit.dtu.dk/ws/files/4151035/Nielsen.pdf
12. Masashi I. Performance Comparison between Self-timed Circuits and Synchronous Circuits Based on the Technology Roadmap of Semiconductors [Electronic resource] / I. Masashi, N. Takashi. – Access mode: http://webhost.laas.fr/TSF/WDSN08/2ndWDSN08(LAAS)_files/Texts/WDSN08-05-Imai.pdf
13. Kenny R. The Breakthrough Advantage for FPGAs with Tri-Gate Technology [Electronic resource] / R. Kenny, J. Watt. – Access mode:URL:https://www.altera.com/en_US/pdfs/literature/wp/wp-01201-fpga-tri-gate-technology.pdf
14. Tyurin S. F. LUT based Fredkin gate / S.F. Tyurin // Radio Electronics, Computer Science, Control. – 2020. – № 1. – P. 44–53.
15. Improving of a Circuit Checkability and Trustworthiness of Data Processing Results in LUT-based FPGA Components of Safety-Related Systems // [A. V. Drozd, M. Drozd, O. Martynyuk, M. Kuznietsov]. – CEUR Workshop Proceedings. –2017. – Vol. 1844. – P. 654–661.
16. Drozd A. V. Use of Natural LUT Redundancy to Improve Trustworthiness of FPGA Design / A. V. Drozd, M. Drozd, M. Kuznietsov // CEUR Workshop Proceedings. – 2016. – Vol. 1614. – P. 322–331.
17. Speedster22i Configuration User Guide [Electronic resource]. – Access mode: http://www.achronix.com/wp-content/uploads/docs/Speedster22i_Configuration_User_Guide_UG033.pdf
18. Maheswaran K. Hazard-free implementation of the self-timed cell set in a Xilinx FPGA [Electronic resource] / K. Maheswaran, V. Akella. – Access mode: http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.39.4276&rep=rep1&type=pdf
19. Osuna C. G. A Self-Timed Multipurpose Delay Sensor for Field Programmable Gate Arrays (FPGAs) [Electronic resource] / C. G. Osuna, P. Ituero and M. López-Vallejo. – Access mode: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC3926550/
20. National Instruments [Electronic resource]. – Access mode: // http://www.ni.com/multisim/
21. Microwind & Dsch Version 3.5 [Electronic resource]. – Access mode: http://auto.teipir.gr/sites/default/files/microwind_manual_lite_v35.pdf
22. Tyurin S.F. Investigation of a Hybrid Redundancy in the Fault-Tolerant Systems/ S. F. Tyurin // Radio Electronics, Computer Science, Control. – 2019. – № 2. – P. 23–33. DOI: 10.15588/1607-3274-2019-2-3
23. El-Maleh A. H. Transistor-Level Defect Tolerant Digital System Design at the Nanoscale. Research Proposal Submitted to Internal Track Research Grant Programs [Electronic resource] / A. H. El-Maleh, A. Al-Yamani, B. M. Al-Hashimi. – Access mode: http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.474.3844&rep=rep1&type=pdf
24. Mead C. A. Introduction to VLSI Systems [Electronic resource] / C. A. Mead, L. Conway. – Access mode: https://www.researchgate.net/publication/234388249_Introduction_to_VLSI_systems

DOI 10.15588/1607-3274-2021-1-4