ASIAN - Self-Timed Logic Circuits Analysis Subsystem

Abstract

Subject of the report - the analysis of the asynchronous circuits independence behaviour from the element delays. Such circuits are known as self-timed. The circuit is defined as the boolean equation sets (logic elements), satisfying to delays Maller hypothesis. The analysis is based on the transition diagram constructions covering all possible scheme states, and known as global state circuit analysis methods. The main advantage of these methods consists in their universality – opportunities of application for the all self-timed circuit class analysis. Subsystem ASIAN is the program complex, which have allowed repeatedly to reduce a time expense for the analysis procedure in comparison by existing analogues and, in essence, to realize the greatest possible analysis efficiency.