

Self-timed multiplier for multiply-add unit

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Content

- **Self-timed (ST) multiplier**

ST coding for data signals

Circuitry of the ST multiplier

Wallace-tree for ST multiplier

- **Layout**

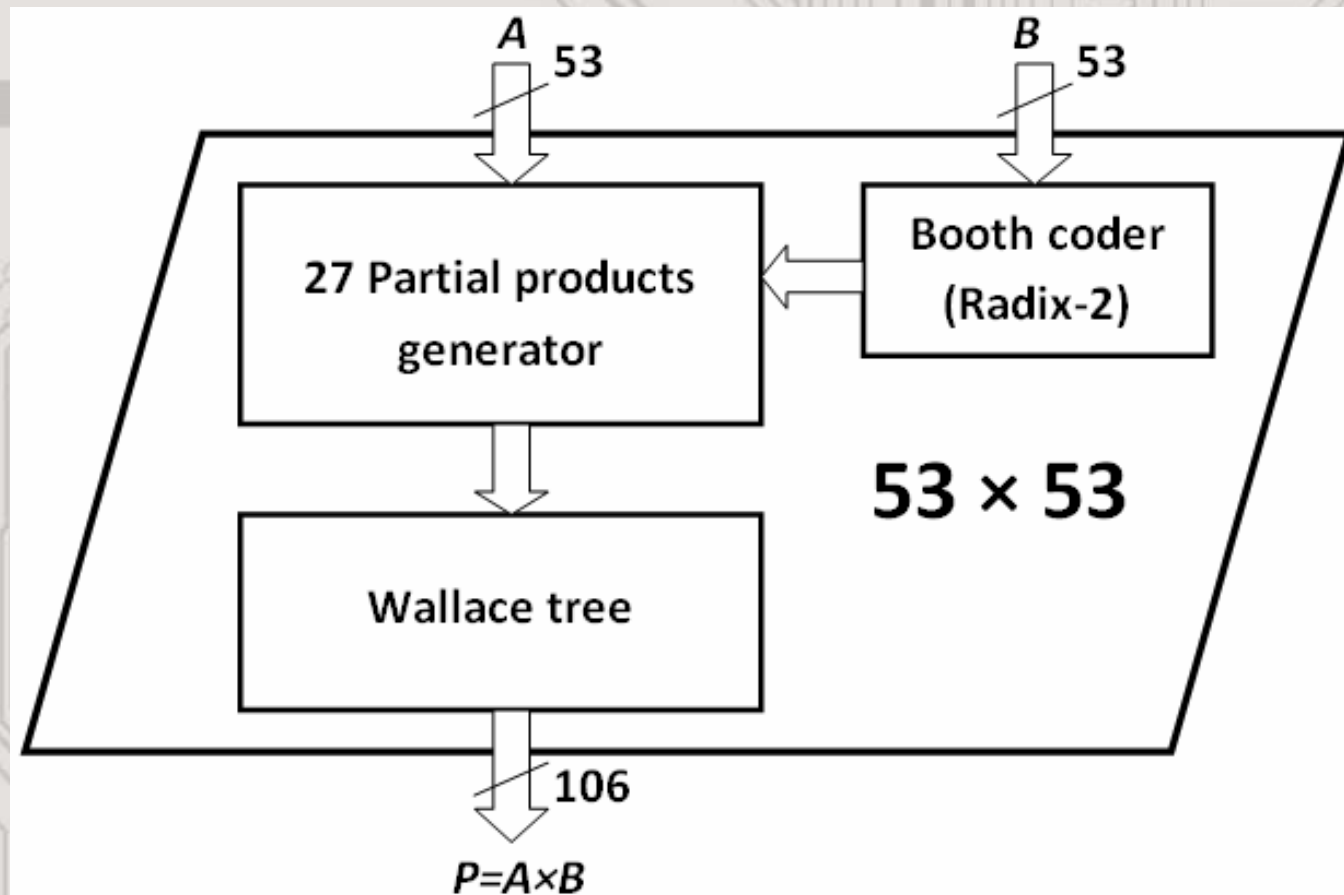
Layout of the 1-bit ternary adder

Layout of the multiplier

Self-timed (ST) circuits

- **Advantages:** low power consumption, self-test, high performance.
- **Disadvantages :** design complexity, higher hardware costs, excessive number of signals in the circuits

Flow-chart of 53x53 multiplier



Comparison of coding methods

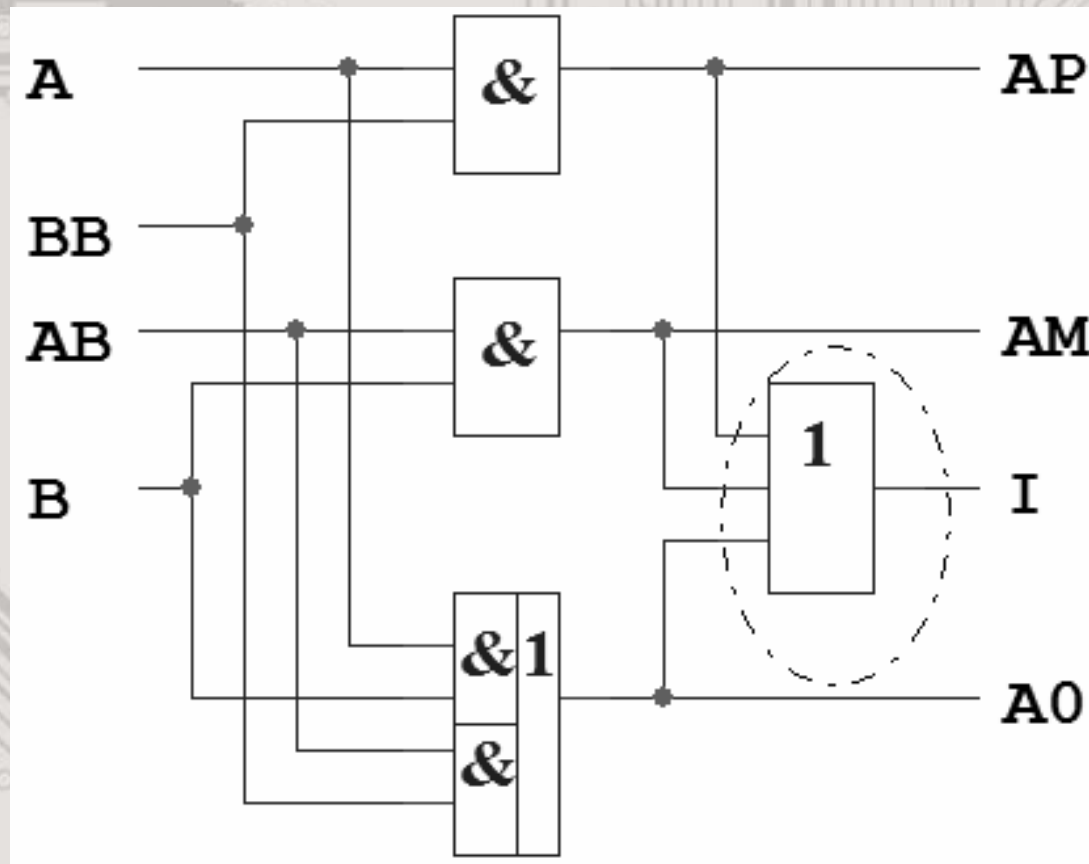
TABLE I. SYNCHRONOUS BINARY CODE

Coded state	Binary code	
	<i>A</i>	<i>B</i>
+1	1	0
0	0	0
-1	0	1
unused	1	1

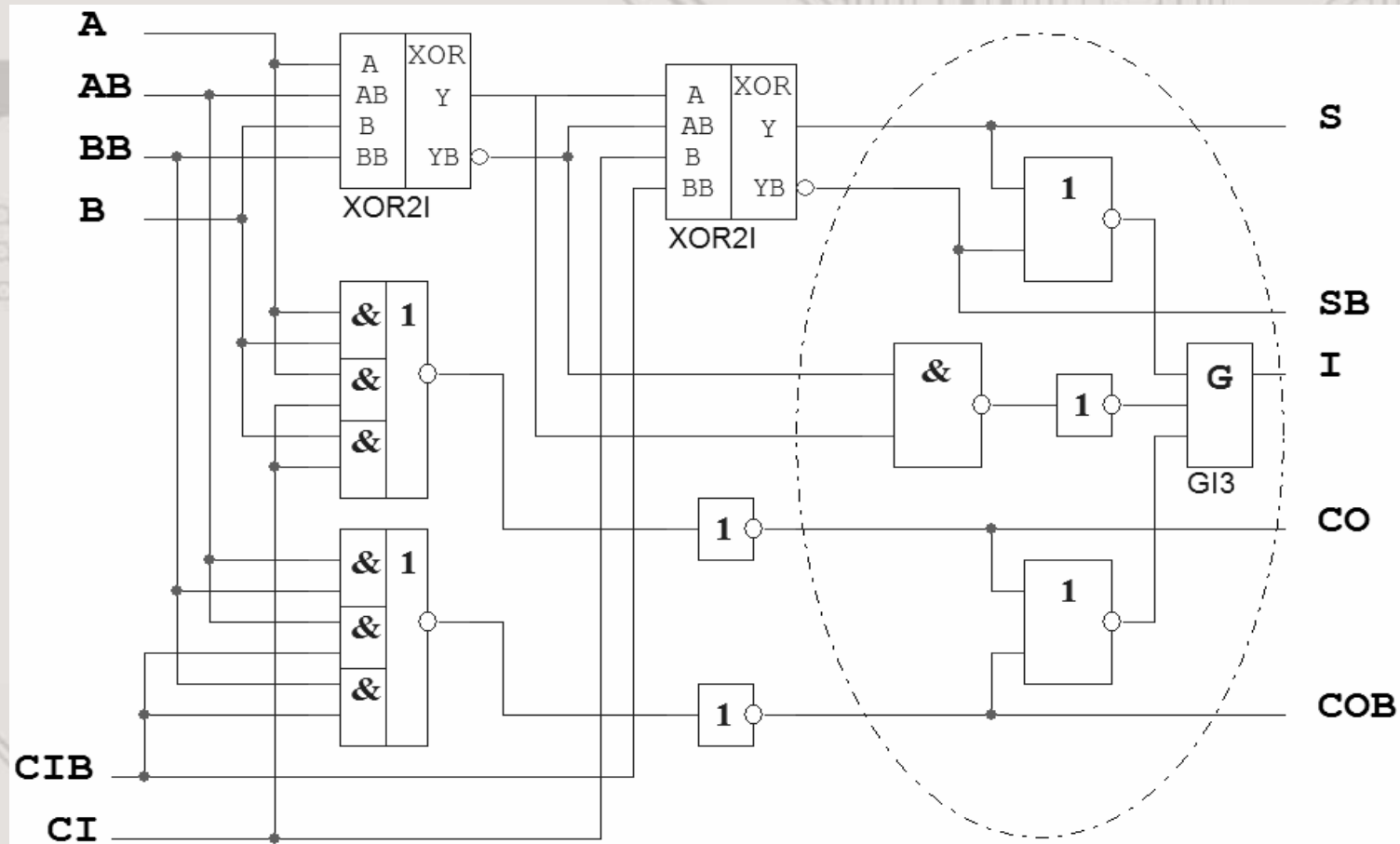
TABLE II. ST TERNARY CODE

Coded state	Ternary code		
	<i>Ap</i>	<i>Am</i>	<i>An</i>
+1	1	0	0
0	0	0	1
-1	0	1	0
spacer	0	0	0

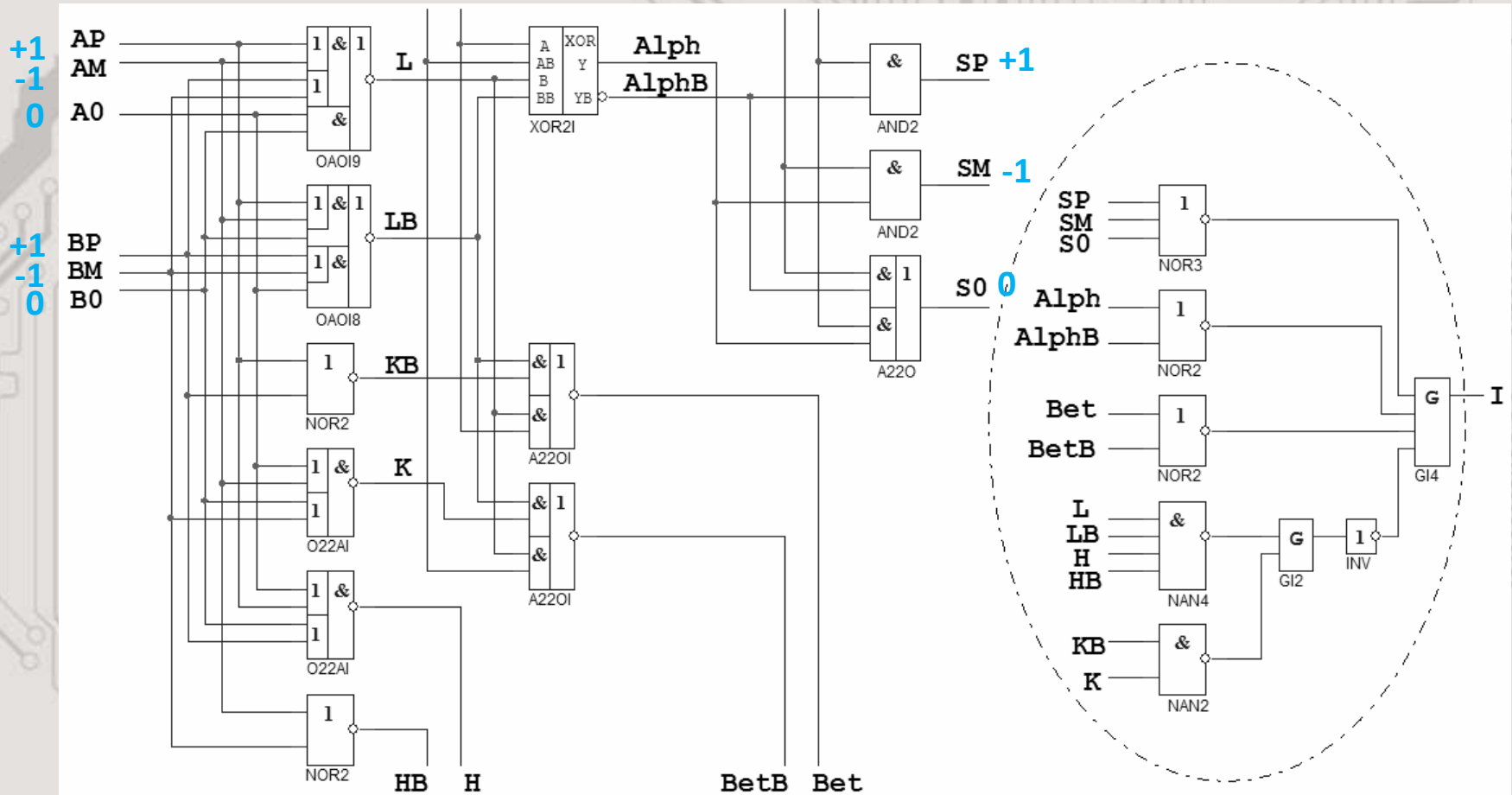
Dual-rail pair to ternary signal converter



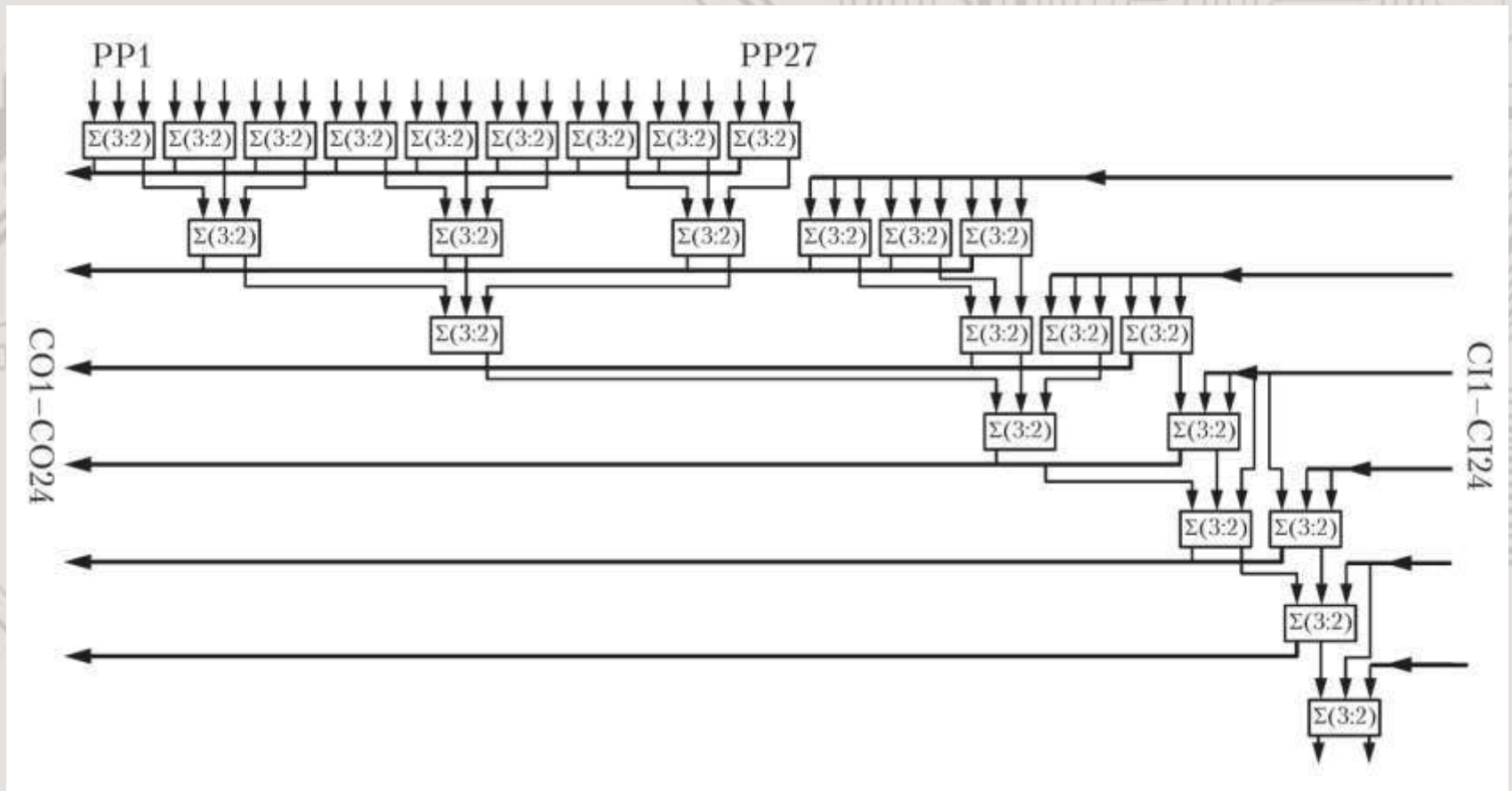
Dual-rail ST adder (78 transistors) 3:2



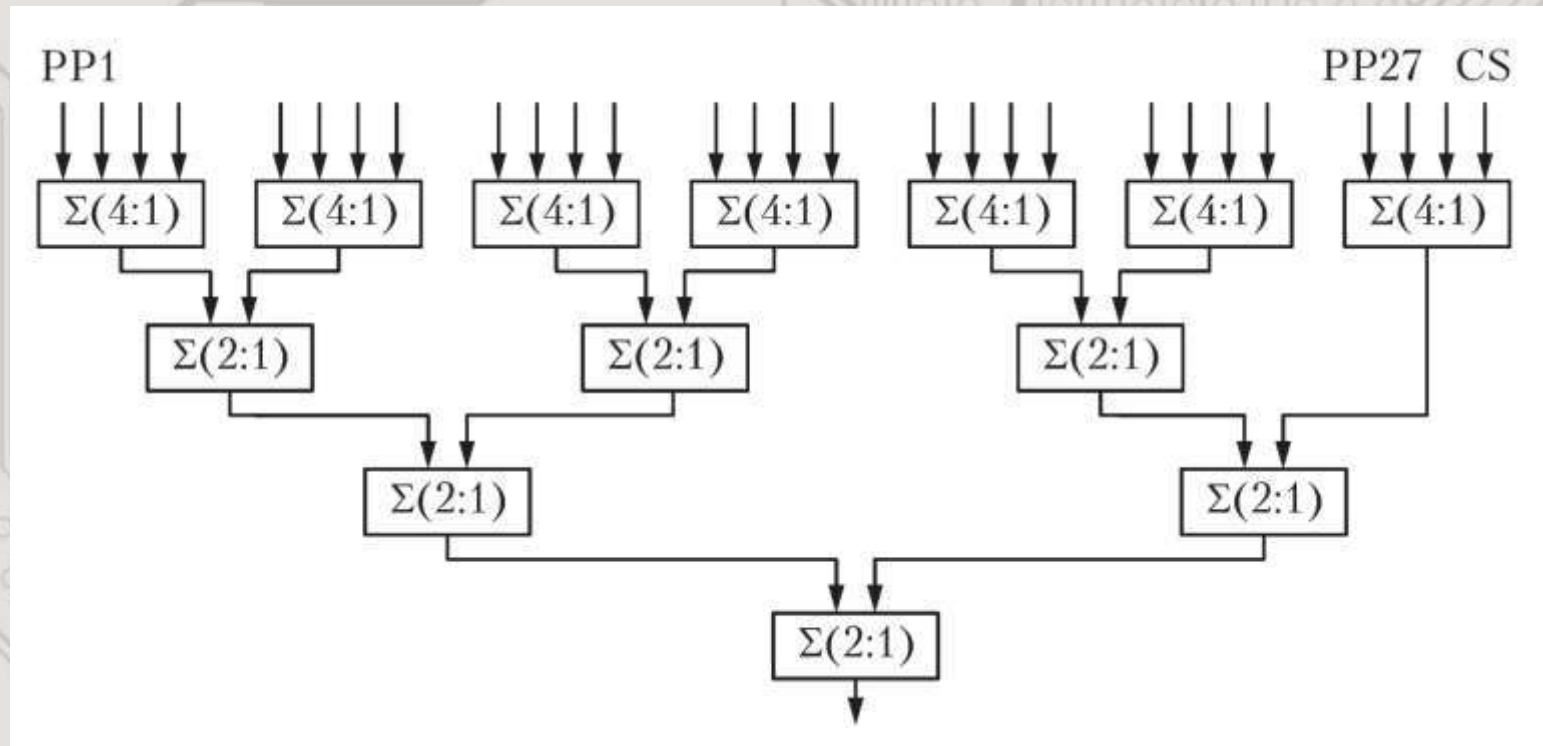
Ternary ST adder (154 transistors) 2:1



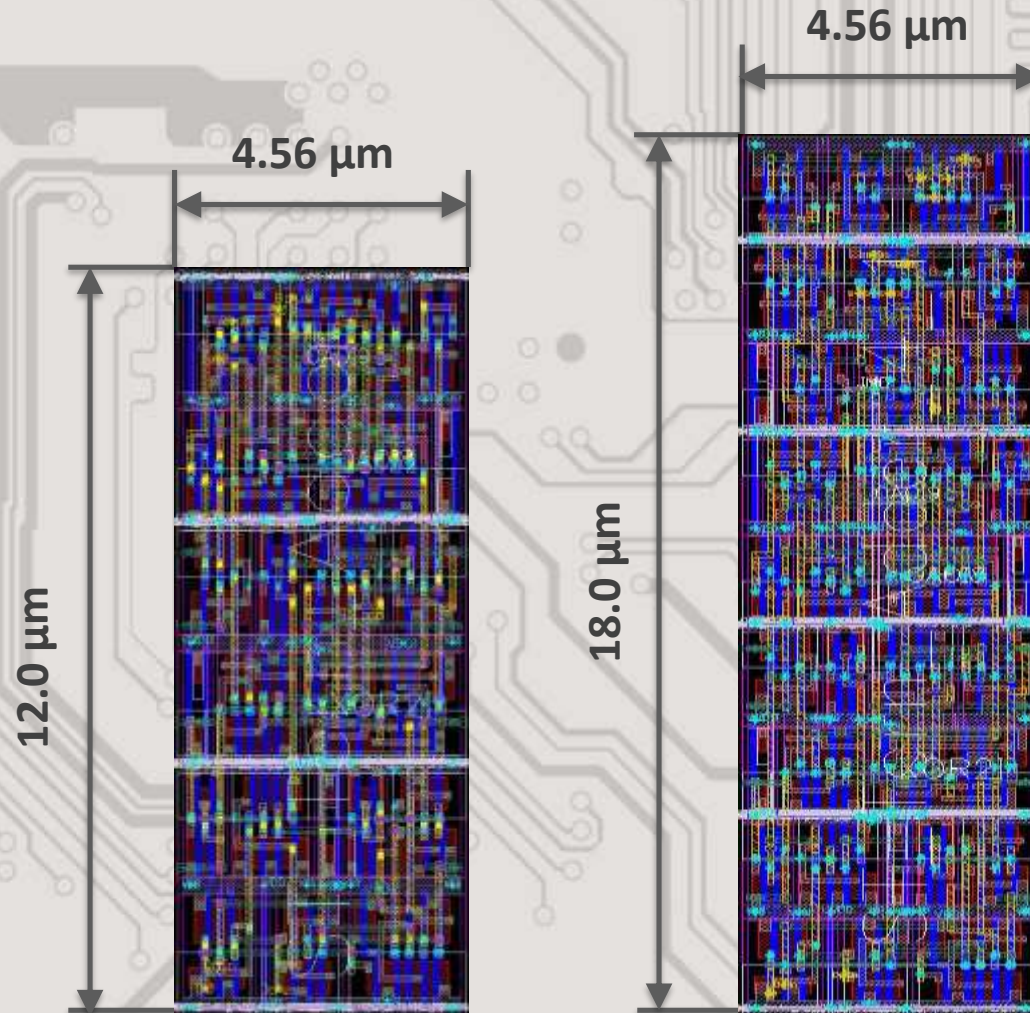
Dual-rail ST implementation of the Wallace tree



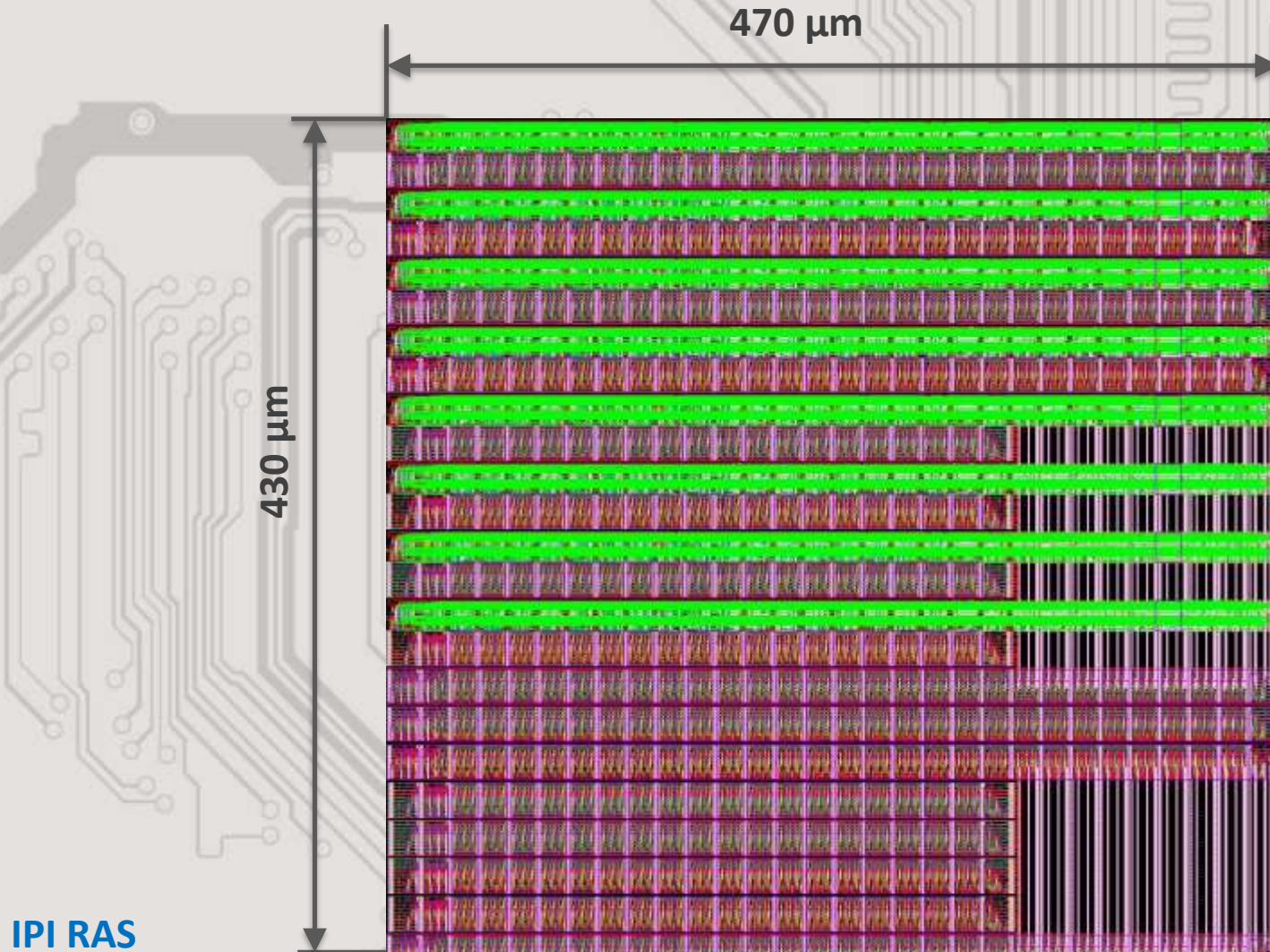
Ternary ST implementation of the Wallace tree



Layout of the 1-bit ternary adder 2:1 and 4:1



Layout of the multiplier



Conclusions

- **ST Multiplier has the evident advantages in comparison with synchronous analogs:**
 - Reducing number of stages of the Wallace tree
 - Wider workability range on supply voltage and temperature
 - Detect, and locate constant failures, allowing circuit self-repairing in real time
- **Layout structure with a vertical propagation of signals simplifies signal routing in the circuit**

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