Self-Timed Multiply-Add-Subtract Unit Alternates

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Content

- FMAS – What is It?
- Ternary FMAS Alternates
- Dual-Rail FMAS Alternate
- Multiplier Alternates
- Comparison of All Alternates
- Conclusion

Fused Multiply-Add-Subtract (FMAS) Unit

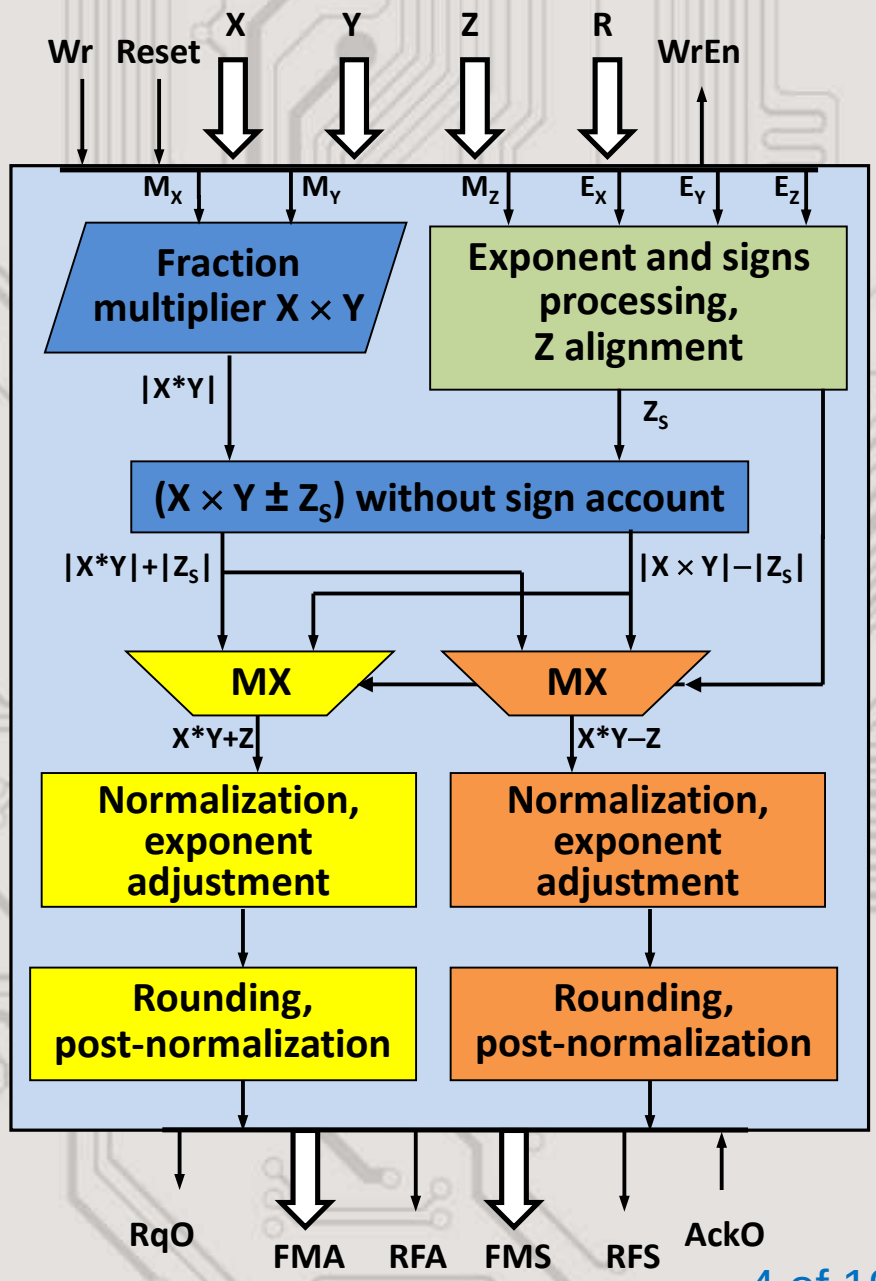
- **IEEE754 Standard**
- **Performed functions :**

  FMA = X × Y + Z,

  FMS = X × Y – Z
- **Precision:**
  - **Double - one 64-bit operation,**
  - **Single - two 32-bit operations**

Block-diagram of the FMAS

X, Y, Z – input operands;
R – operation options;
FMA, FMS – results;
RFA, RFS – result flags;
Wr – write;
WrEn – write-enable;
RqO – output request;
AckO – output acknowledge



Ternary & Quaternary Encoding

Number	Ternary code			Quaternary code			
	AP	AM	A0	AP	AM	A0	A0N
+1	1	0	0	1	0	0	1
0	0	0	1	0	0	1	0
–1	0	1	0	0	1	0	1
spacer	0	0	0	0	0	0	0

Ternary & Quaternary Multipliers

Modified Booth Algorithm:

S_i – dual-rail partial products;

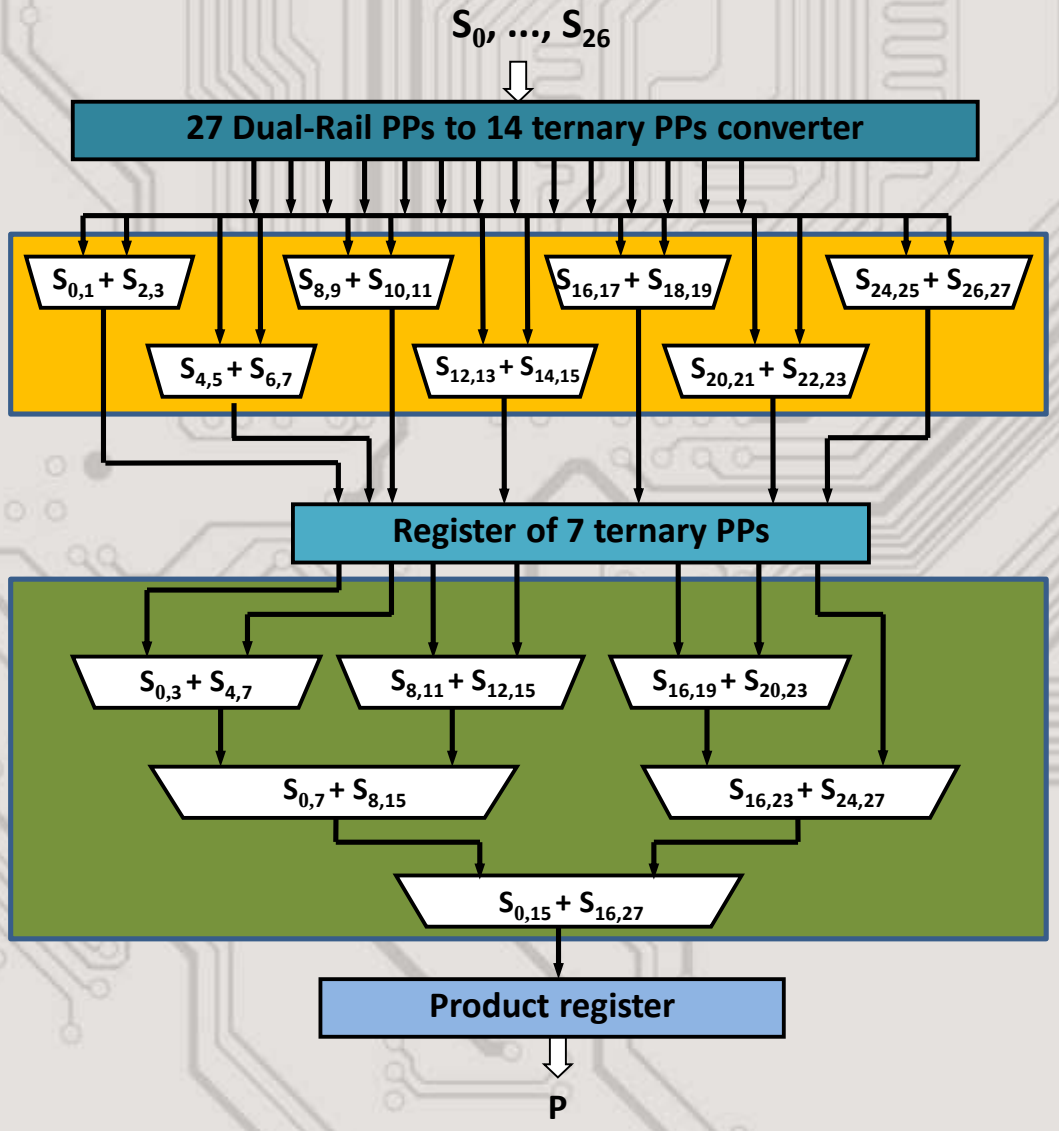
$S_{j,k}$ – ternary/quaternary partial products;

P – resulted product.

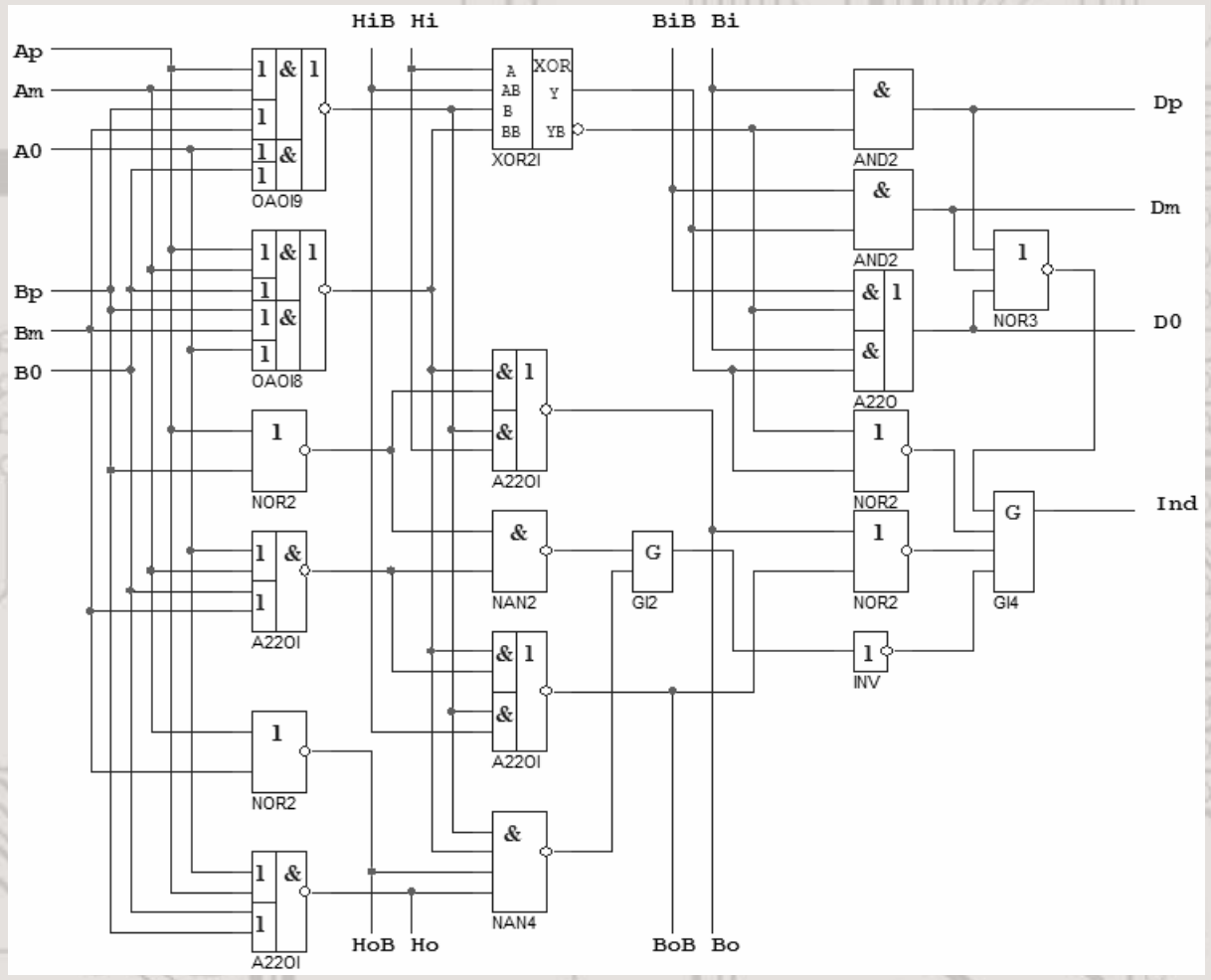
Dual-rail PPs to Ternary PPs converter:

$$S_A + S_B = S_A - \overline{S_B} - 1 = S_{A,B} - 1$$

4 Stages of Wallace Tree

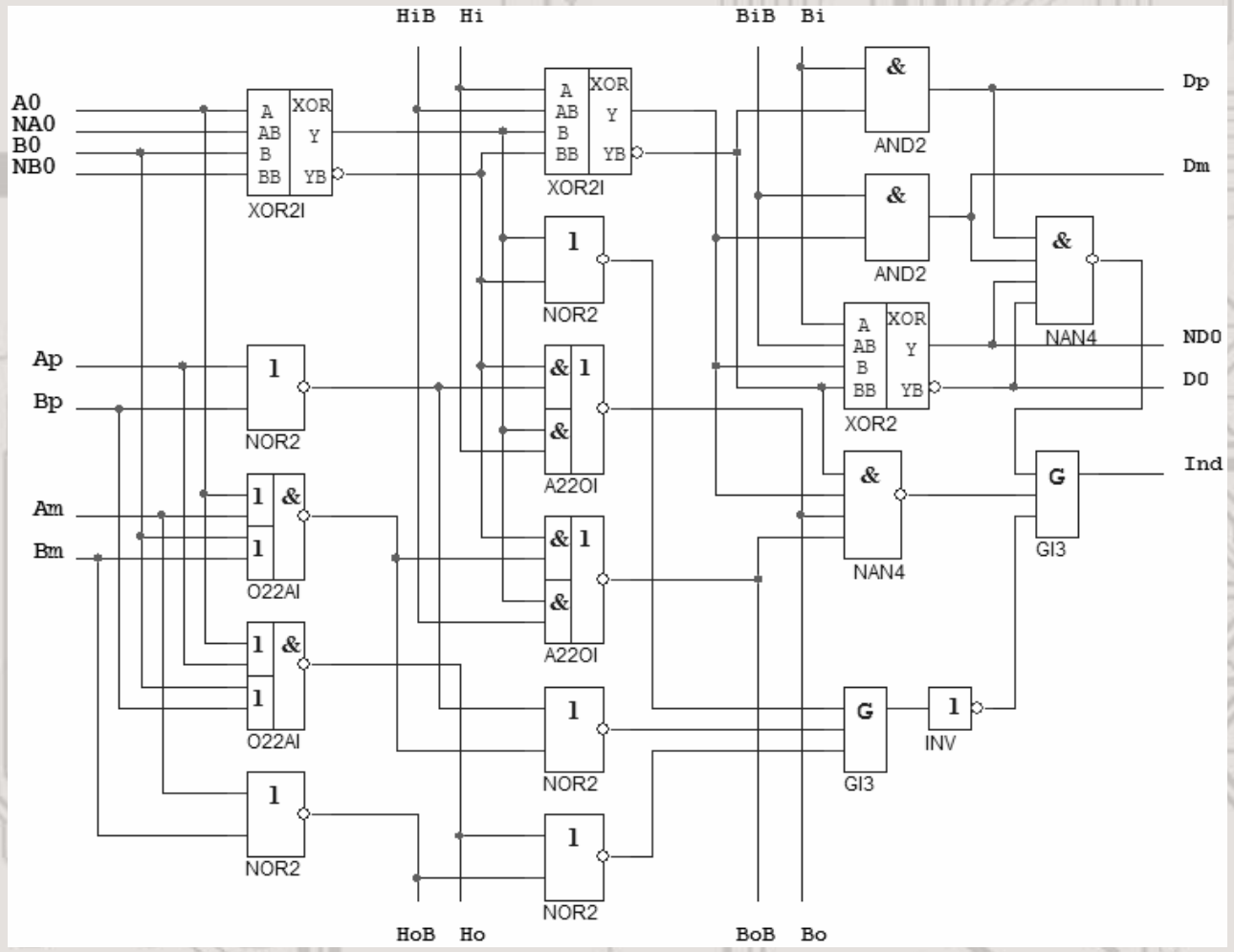


Ternary Self-Timed Adder



158 CMOS transistors; 2:1 Compression

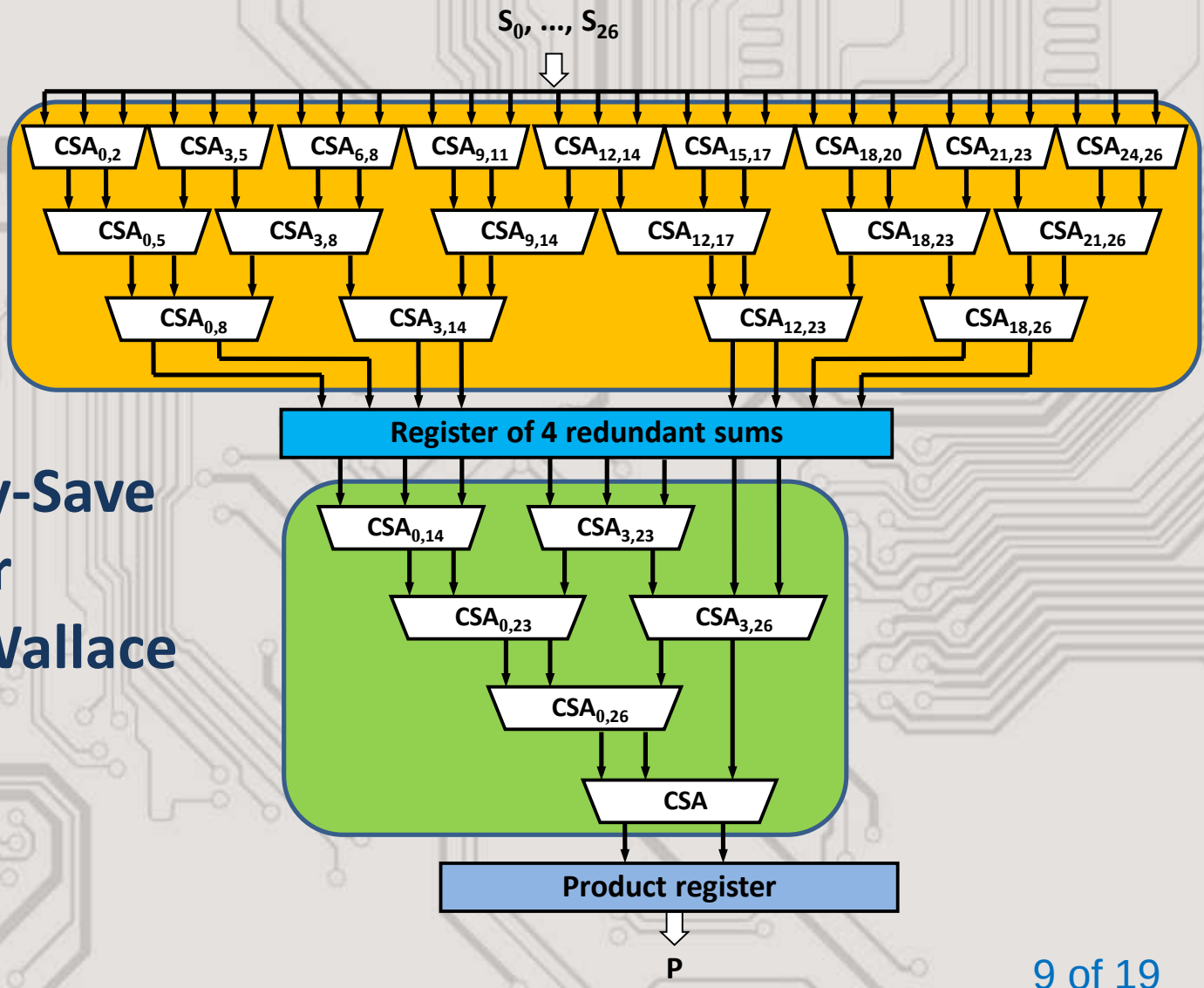
Quaternary Self-Timed Adder



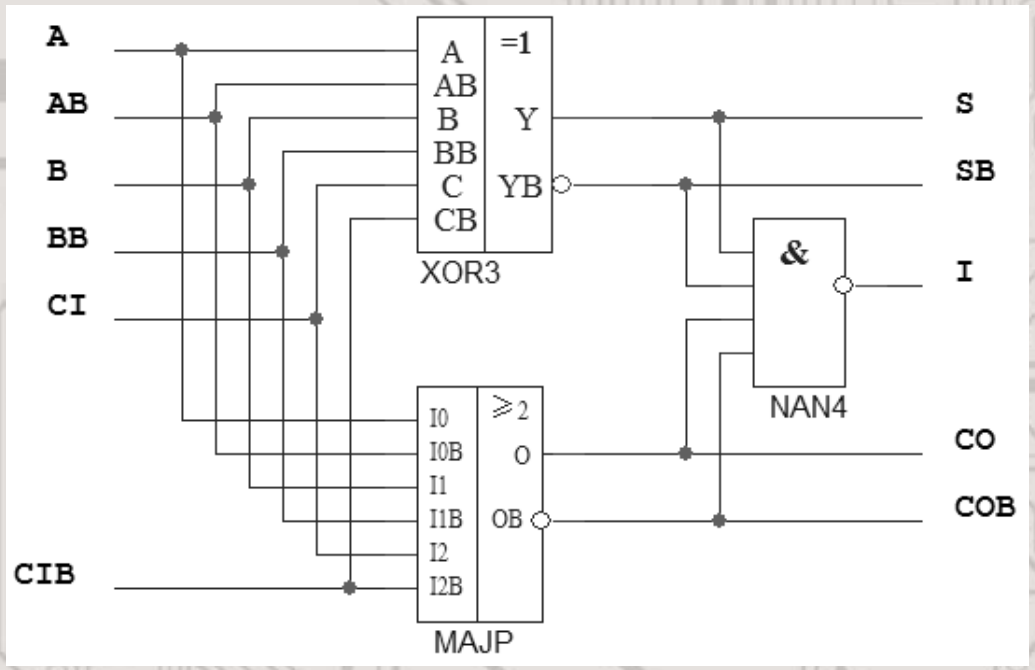
168 CMOS transistors; 2:1 Compression

Dual-Rail Multiplier

- $CSA_{j,k}$ – Carry-Save Adder
- 7 Stages of Wallace Tree



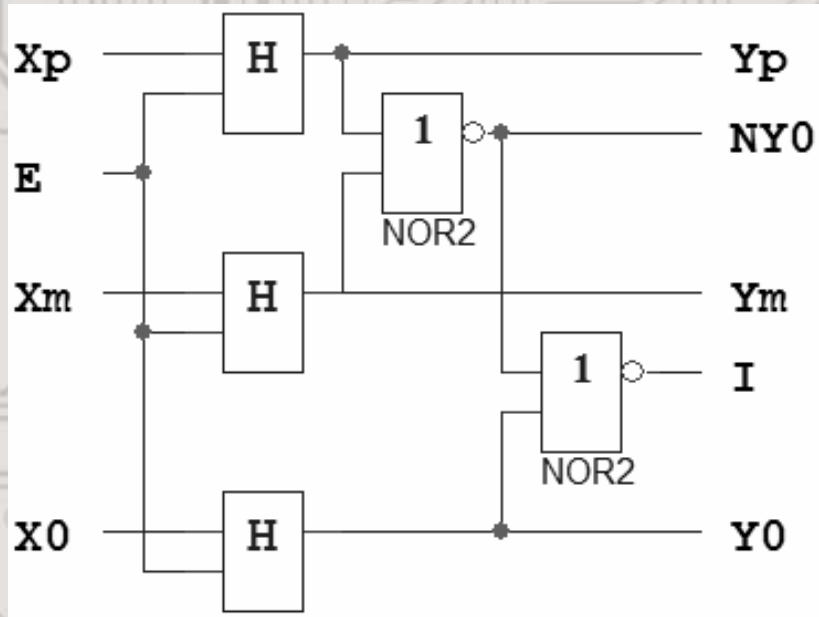
Dual-Rail Self-Timed Adder



- **56 CMOS transistors,**
- **3:2 Compression**

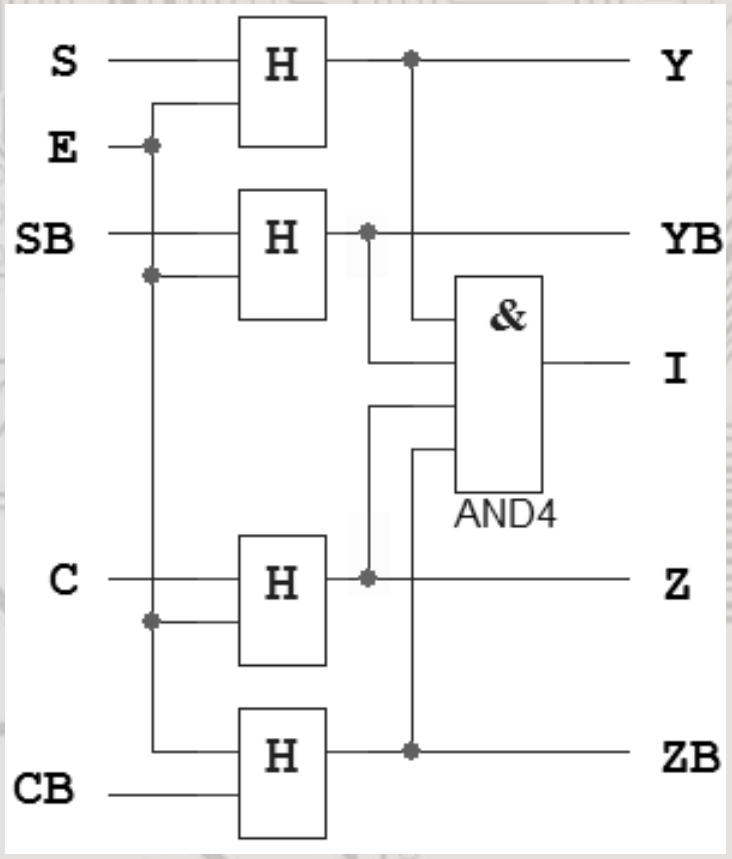
One-Bit Quaternary Register

- **Hysteretic trigger (H-trigger):**
  $Z^{+} = A \cdot B \vee Z^{-} \cdot (A \vee B)$
- **Register stores ternary bit but outputs quaternary data**



One-Bit Dual-Rail Register

- **Register stores redundant representation of the one bit of the dual-rail partial product**



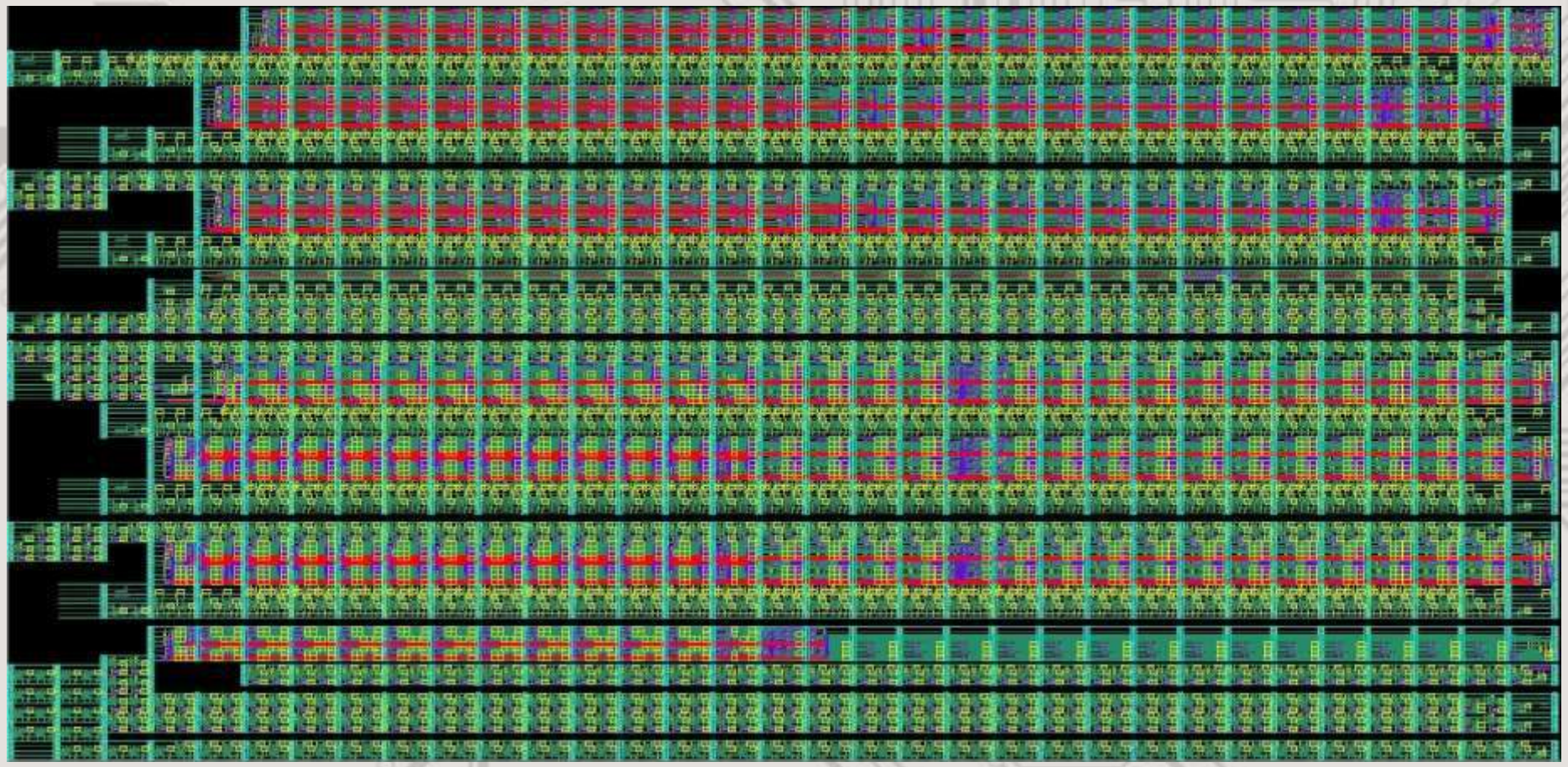
Multiplier Alternates: Complexity, CMOS transistors

Functional Unit	Multiplier Case		
	Ternary	Quaternary	Dual-Rail
Booth coder	3,000	3,000	3,000
Booth decoder	94,000	94,000	94,000
Dual-rail PP sum to ternary PP converter	51,500	54,000	–
Wallace tree	134,000	139,000	85,000
Registers	16,000	17,000	24,000
Indication subcircuit	7,000	7,000	12,000
Total	305,500	314,000	218,000

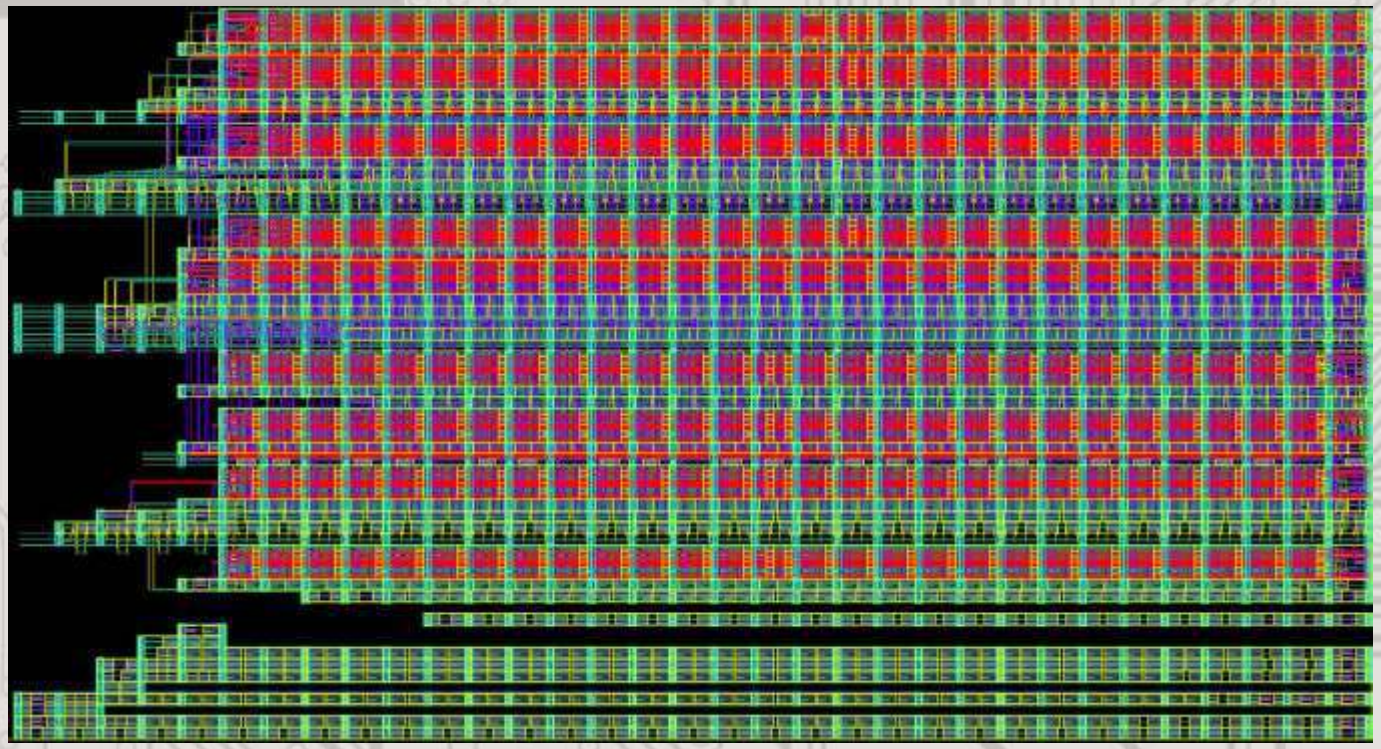
Multiplier Alternates: Cycle Duration, ps

Pipeline Stages	Multiplier Case		
	Ternary	Quaternary	Dual-Rail
1	1,640	1,620	1,390
2	1,200	1,170	1,030

Multiplier Alternates:
Quaternary Layout (630 × 316) μm²



Multiplier Alternates: Dual-Rail Layout (480 × 264) μm²



1.62 times less comparing to quaternary multiplier !

FMAS Alternates: Cycle Duration, ps

Operation Precision	FMAS Alternates		
	Ternary	Quaternary	Dual-Rail
Single	1,350	1,350	1,350
Double	1,350	1,350	1,310

Conclusions

- Due to a simpler implementation of the one-bit dual-rail carry-save adder as compared to the quaternary/ternary self-timed adder, Wallace tree in dual-rail multiplier has 1.44 times less complexity, 13% higher performance, and 1.62 times less layout area implementation than ternary one
- Booth multiplier splitted up into two stages is not the bottleneck of the FMAS pipeline
- The further increase of the pipeline stage number does not affect FMAS performance

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