Speed-Independent Fused Multiply-Add Unit of Gigaflops Rating: Methodological Aspects

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EXTENDED ABSTRACT

Keywords – self-timed circuit, supercomputer, multiply-accumulate, adder, pipeline.

This report contains the approaches to designing self-timed (ST) hardware and discusses the requirements for in-system integration of the synchronous and ST units in a framework of supercomputer by an example of development of Speed-Independed Fused Multiply-Add (SIFMA) unit of gigaflops rating conforming to IEEE 754 Standard. SIFMA performs either one double precision operation, or two simultaneous single precision operations with input operands. Its multiplier utilizes a self-timed ternary coding providing better performance. SIFMA was designed under industrial CMOS 65-nm technology. Depending on implementation, it operates with synchronous or asynchronous environment and provides performance no less than 1 Gigaflops at latency up to 6 ns.

In exaflops class supercomputers having up to hundreds of millions of cores, it is practically necessary to strengthen a hardware support of the tools providing a reliability and validity of the calculation results. ST-circuitry suggested for implementing the basic computing units provides a highly efficient solution for this task. For the first time in domestic and foreign practice, an attempt of developing 64/32-bit SIFMA unit as a circuit, whose behavior does not depend on delays of both the cells and wires right to fan-out point, was made. At developing ST adders and ST multipliers, it is reasonable to use not only dual-rail code but also a ternary ST code. From a variety of the algorithms, one should choose the hardwarily justifiable solutions with a minimal number of the stages requiring an indication of data processing termination. In multibit units, one should use a bitwise indication where it is permissible to decrease a bottleneck number in a pipeline. For maximum performance, it is recommended to implement a hardware multiplier utilizing the Wallace tree for adding partial products as a single stage with two parallel computing units in a counter phase mode, if possible.

Reference to full text: http://www.mes-conference.ru/infoMES/index.php?page=vpaper&code=D589&ls=en

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