Speed-Independent Fused Multiply-Add Unit of Gigaflops Rating: Implementation Variants

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EXTENDED ABSTRACT

Keywords – self-timed circuit, multiplier, adder, subtracter, pipeline, indication.

This report contains the results of development of two releases of Speed-Independed Fused Multiply-Add (SIFMA) unit conforming to IEEE 754 Standard. SIFMA performs either one double precision operation, or two simultaneous single precision operations with three operands. SIFMA was designed under industrial CMOS 65-nm technology. It operates with synchronous and asynchronous environments and provides performance up to 1 Gigaflops at 1.0 volt of supply voltage and 25 Celsius degrees.

Suggested releases of SIFMA perform FMA operation in accordance with IEEE 754 Standard. They refer to the units whose behavior does not depend on element's delay, i.e. Speed-Independed (SI) units. Both releases add a product of first two operands to third one, and subtract the same product from third operand simultaneously. They perform such operations with respect to single triplet of double precision operands or two triplets of single precision operands.

Comparative analysis of both advantages and shortcomings of NULL Convention Logic (NCL) and SI-circuits suggested by Varshavskii V.I. and developed by authors has led to choosing SI-circuits as more preferable. They provide less complexity (up to 4.5 times for binary counter implementation, more than 1.1 times for multiplier 4x4 implementation, up to 2 times for implementation of the simpler logical circuits), greater performance and smaller power consumption.

Synchronous environment release differs from asynchronous environment release by presence of input and output 4-word FIFO. An average performance of both SIFMA releases equals to 1.0 Gigaflops at typical conditions (1.0 volt of supply voltage and 25 Celsius degrees). Power consumption equals to 970 and 1140 mJ/GHz for synchronous and asynchronous release respectively. Now both SIFMA releases are being manufactured as a part of test VLSI.

SIFMA was designed on a base of self-timed extension of the TSMC 65-nm standard cell library. Its cells are a subset of a cell library developed by authors and intended for designing self-timed circuits. They were worked through developing SI-coprocessor.

Reference to full text: http://www.mes-conference.ru/infoMES/index.php?page=vpaper&code=D586&ls=en

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