Self-timed multiplier for multiply-add unit

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Abstract

Paper discusses the peculiarities of self-timed multiplier implementation for unit multiplying two operands and then adding the product to third operand without an intermediate rounding according to the IEEE 754 Standard. The multiplier is a hardware implementation of modified Booth algorithm on a base of self-timed adder with redundant signal code. An optimal self-timed redundant coding of internal and output signals in the multiplier was proposed. The circuitry and layout problems were solved for self-timed multiplier implementation. Wallace tree structure, which is the main part of the multiplier, was optimized for the facilities of 65-nm CMOS process with six metal layers taking into account more number of signals in the multiplier circuit, than in the synchronous analog. A release of the self-timed multiplier implementation in CMOS process with 65-nm design rules is introduced.