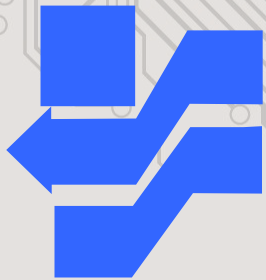


Energy Efficient Speed-Independent 64-bit Fused Multiply-Add Unit

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Academy of Sciences**

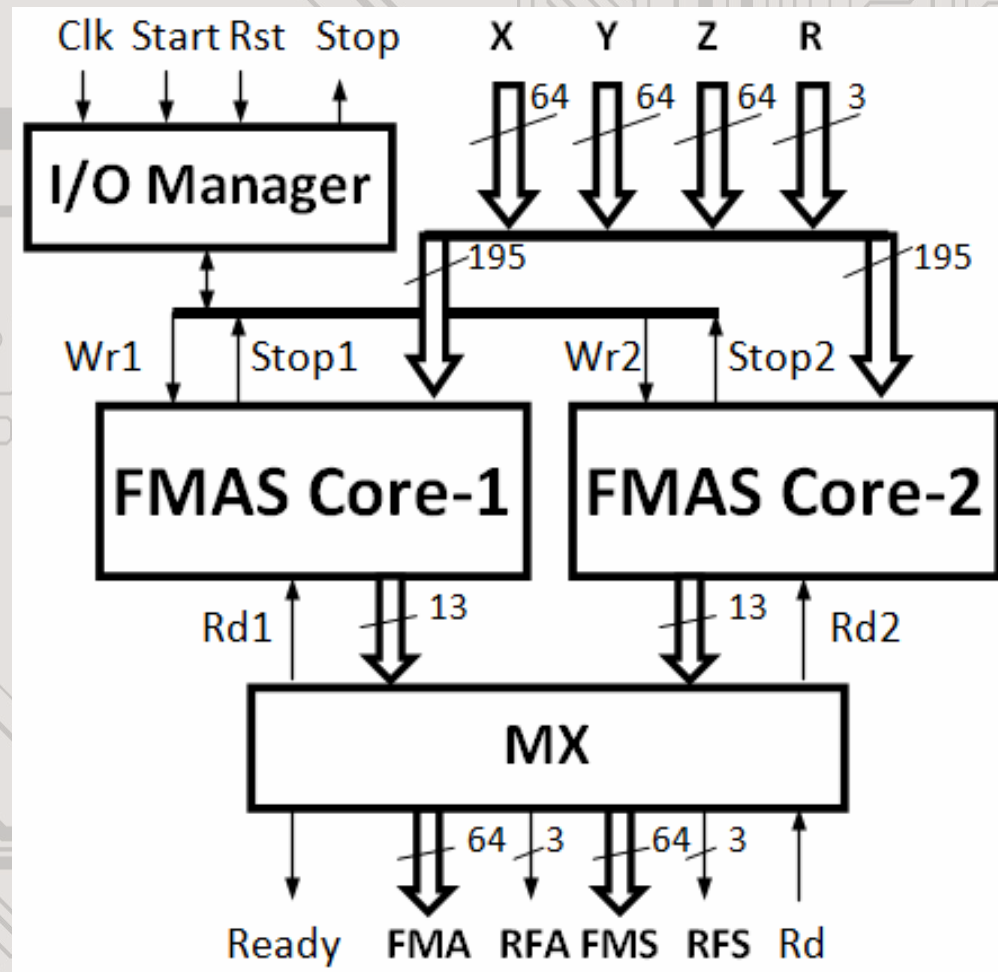
Content

- **Features of the Speed-Independent circuits**
- **Flowchart of the Speed-Independent FMA**
- **Ways for increasing FMA performance**
- **Pipelining multiplier**
- **Input and output FIFO implementation**

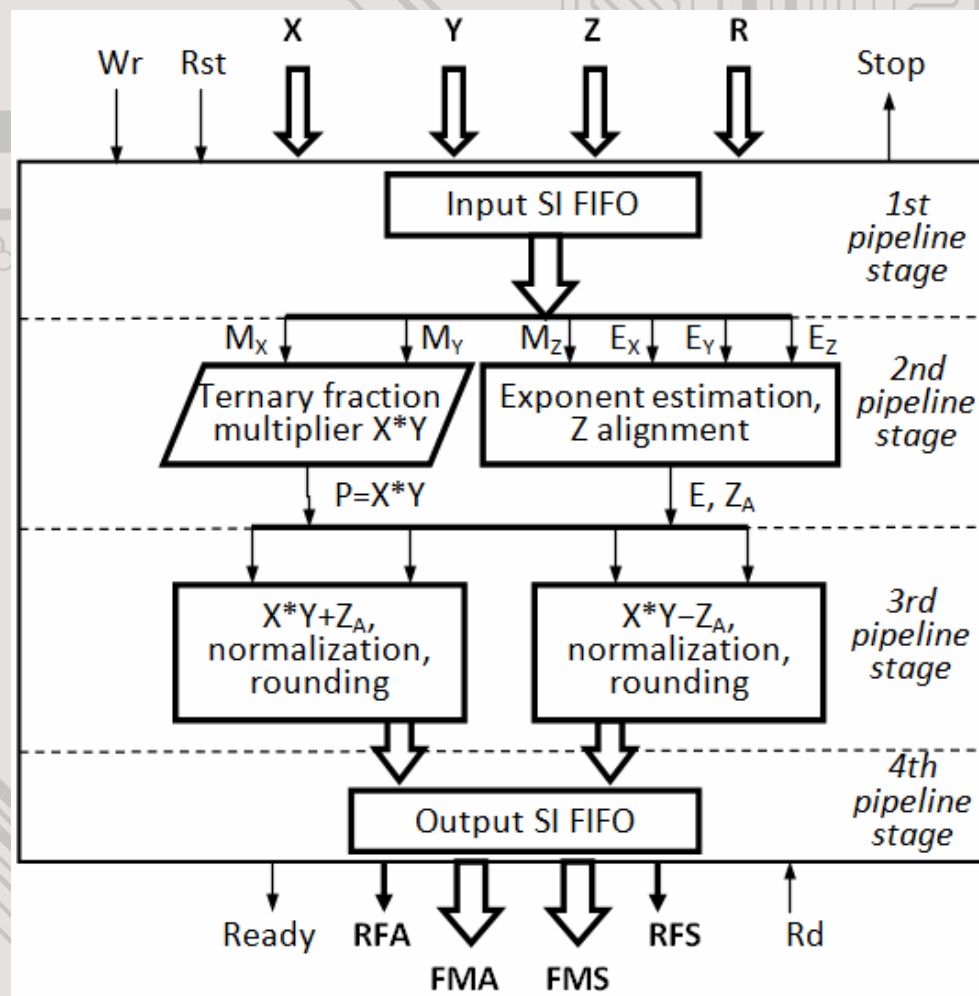
Speed-independent (SI) circuits

- **Advantages:**
 - lack of hazards,
 - self-testing,
 - real performance,
 - wide workability range.
- **Disadvantages :**
 - design difficulty,
 - higher hardware costs,
 - increased number of signals

Flow-chart of previous SI FMA



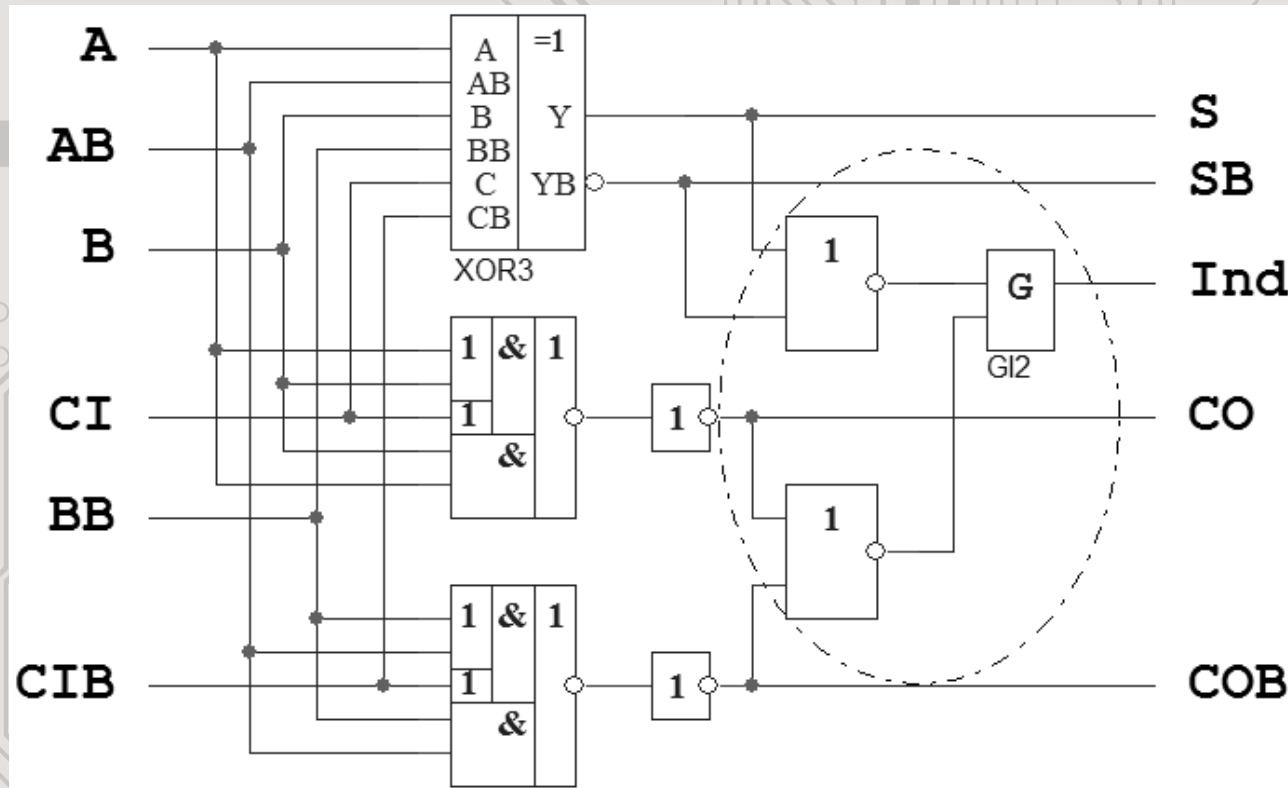
Flow-chart of new SI FMA



Quaternary encoding

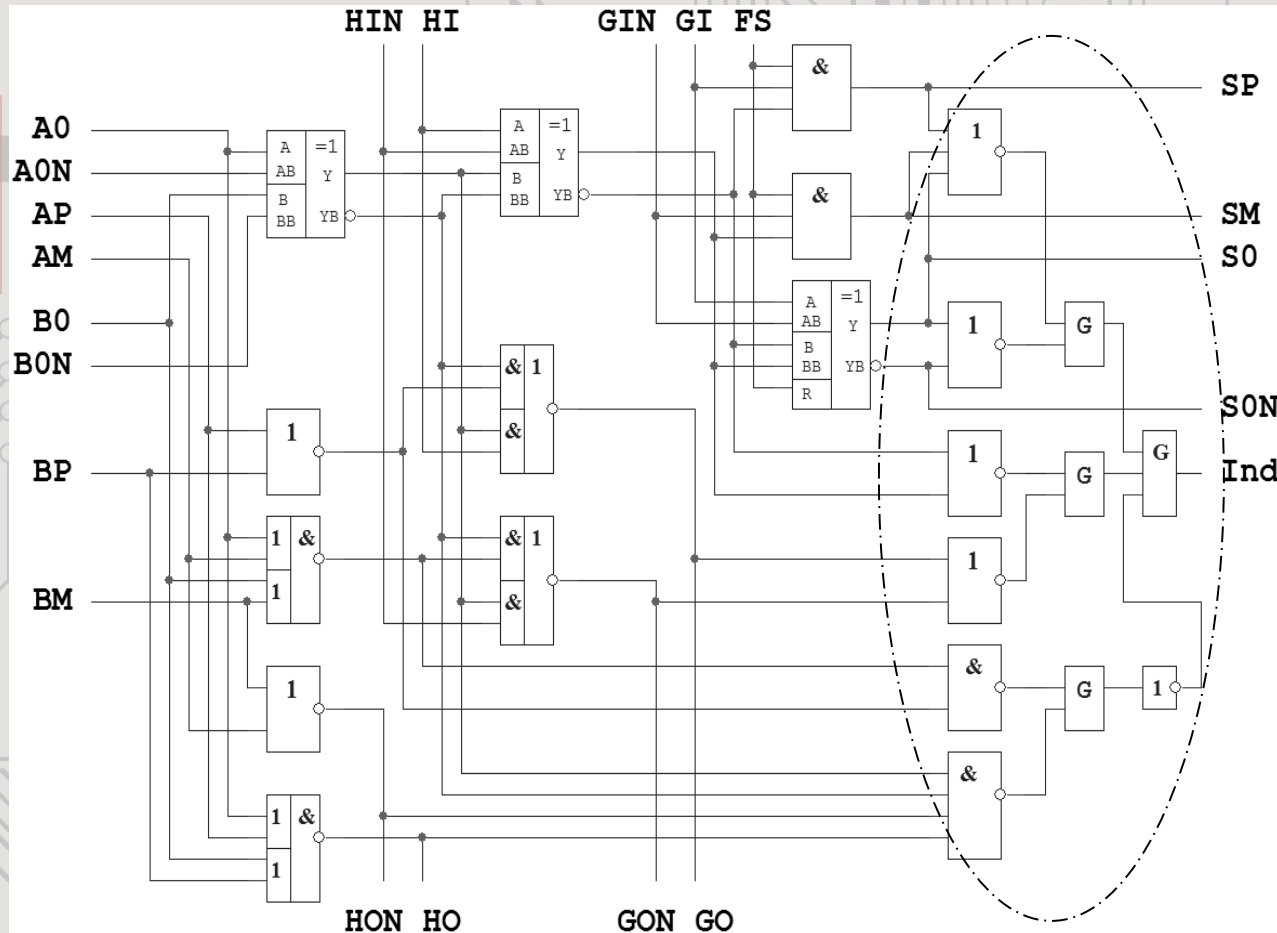
Number	Binary redundant code		Quaternary code			
	A	B	AP	AM	A0	A0N
+1	1	0	1	0	0	1
0	0	0	0	0	1	0
-1	0	1	0	1	0	1
spacer	—	—	0	0	0	0

Dual-rail SI adder



- 68 CMOS transistors,
- 3:2 Compression

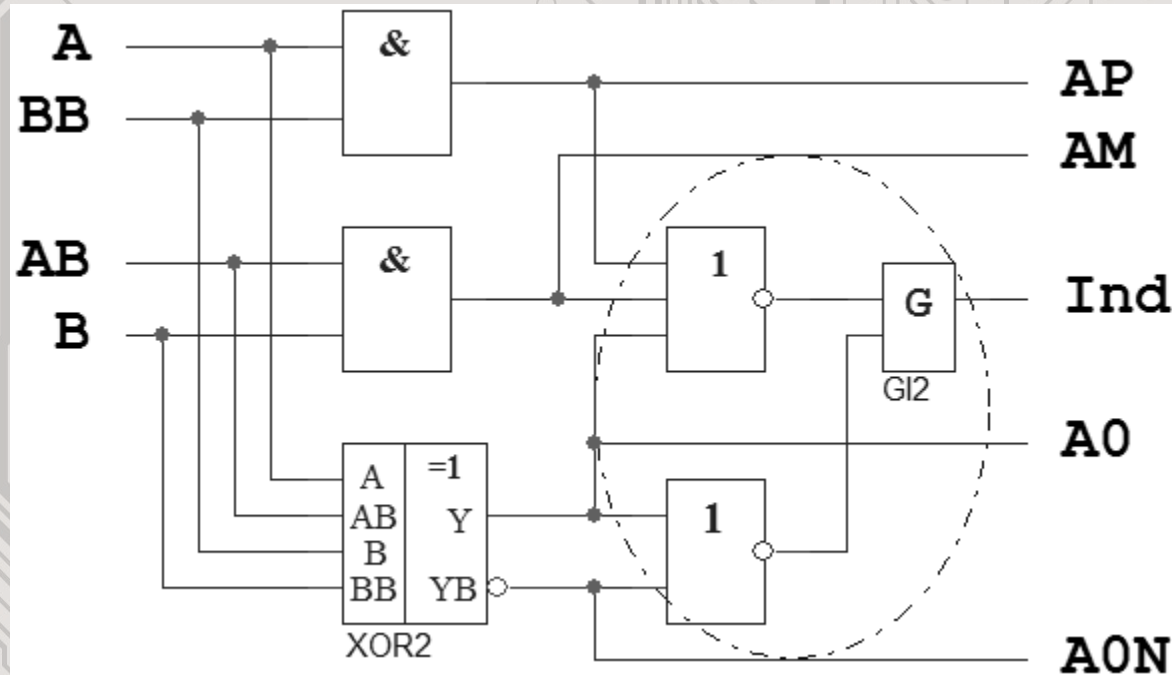
Quaternary SI adder



180 CMOS transistors; 2:1 Compression

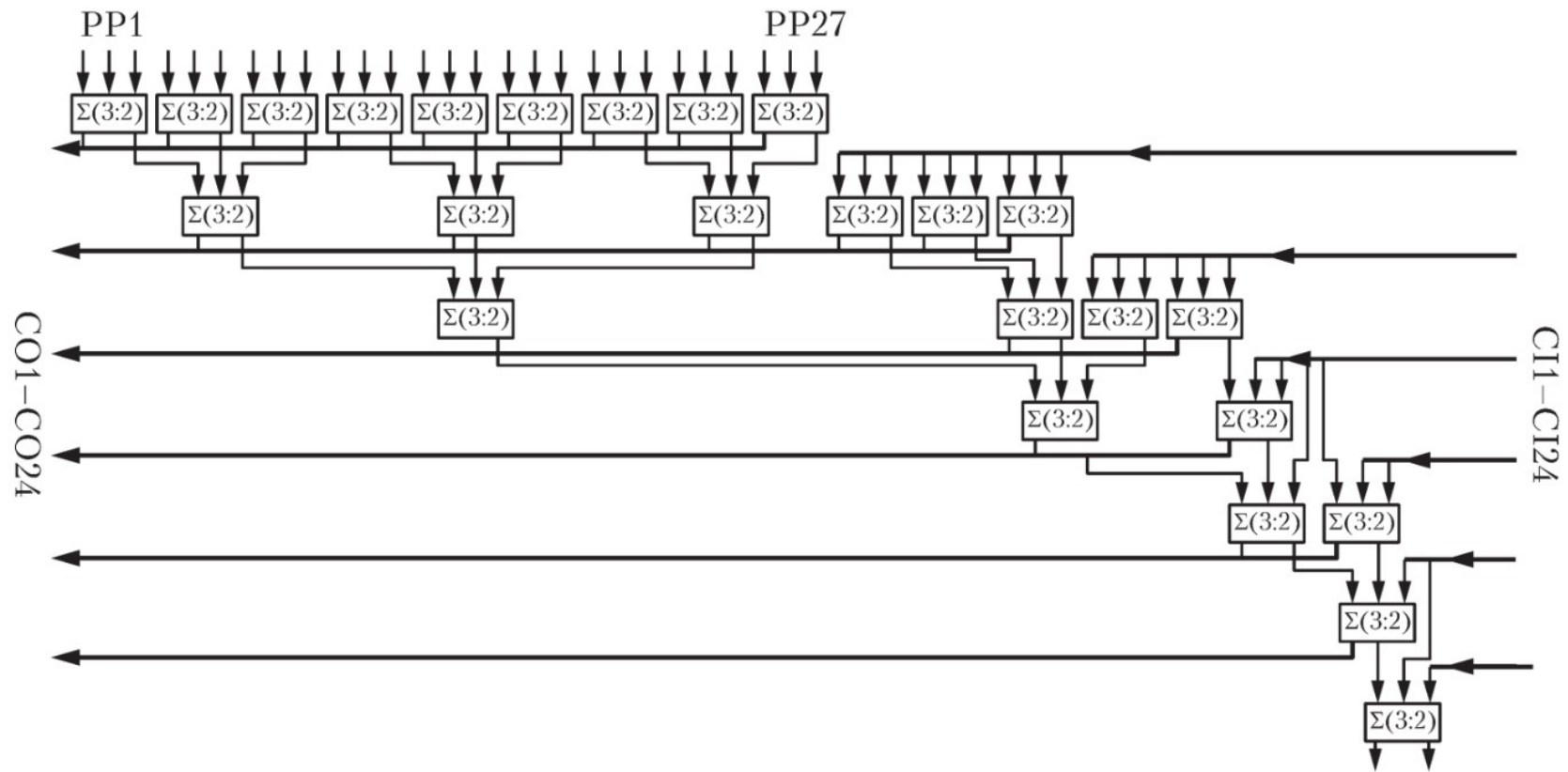
Two Dual-Rails to Quaternary converter

$$\{A, AB\} - \{B, BB\} = \{AP, AM, A0, A0N\}$$

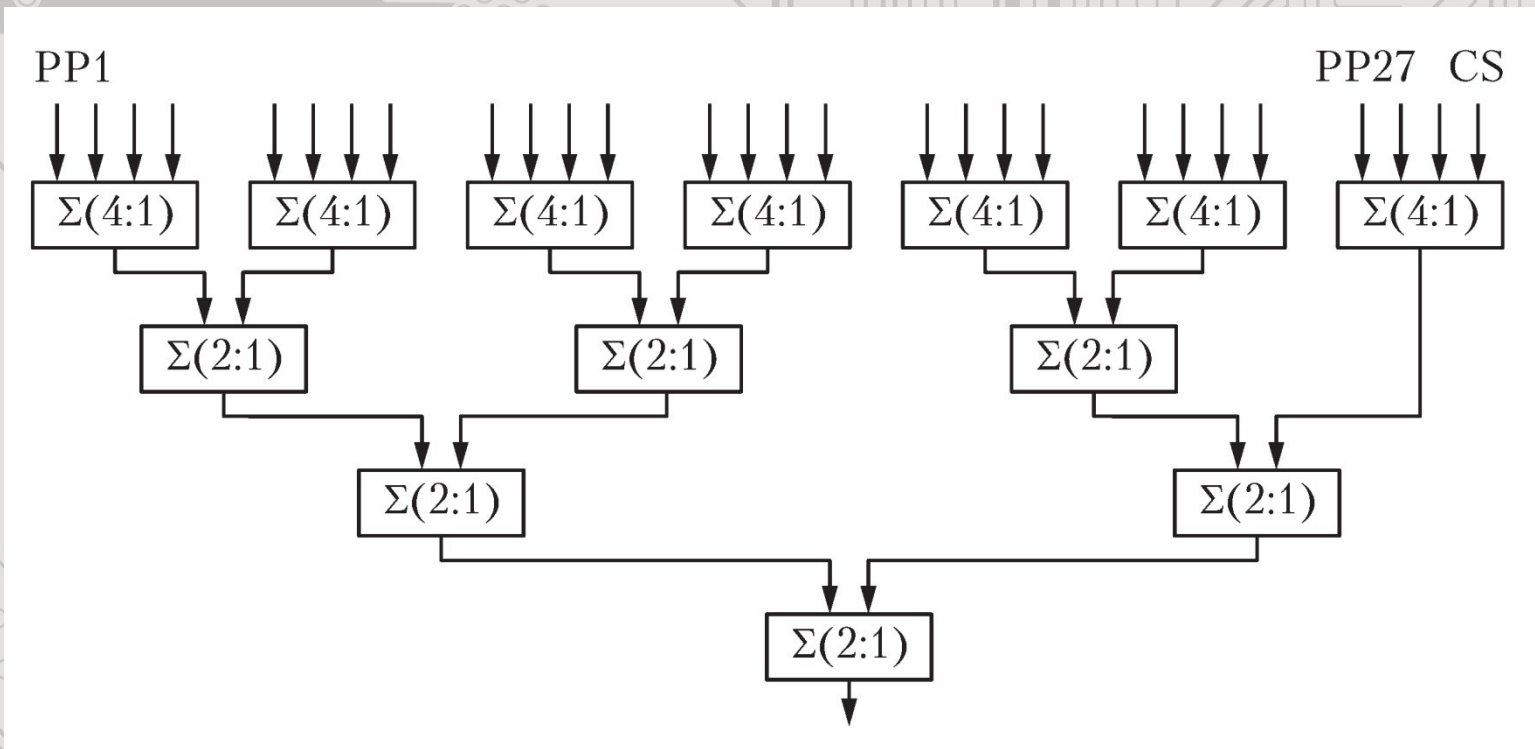


48 CMOS transistors

Dual-rail SI implementation of the Wallace tree: 7 Stages



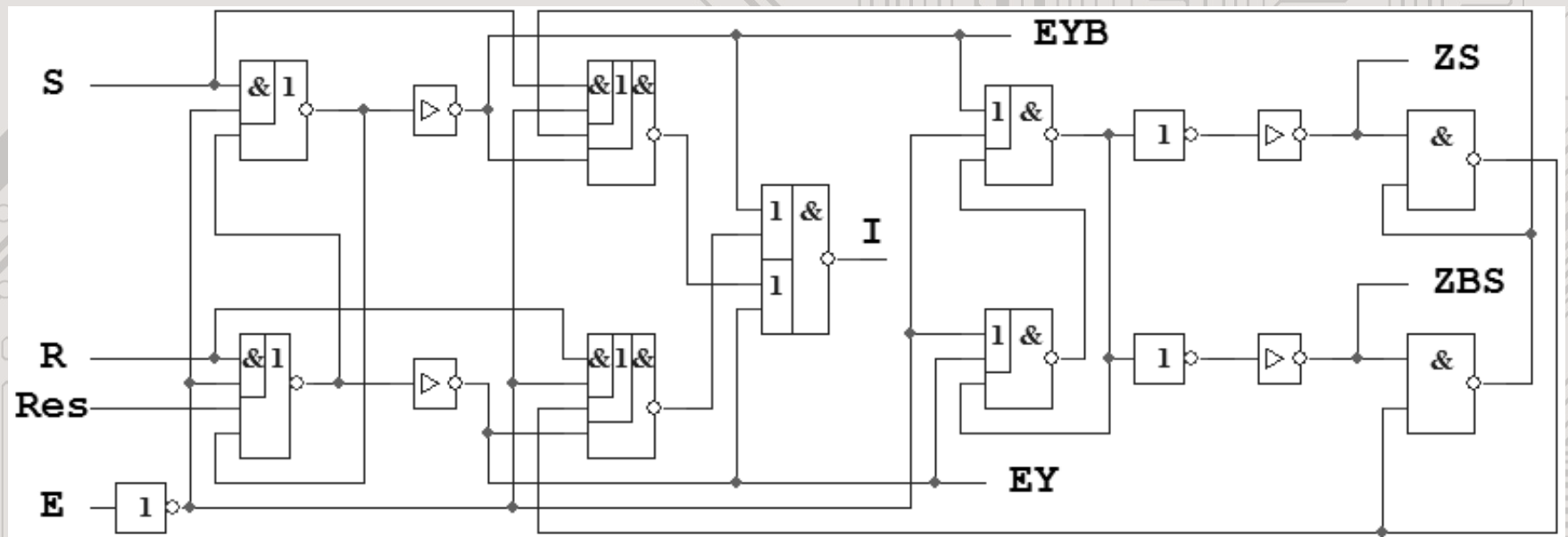
Quaternary SI implementation of the Wallace tree: 4 Stages



Acceleration techniques

- **Forced transition of the Wallace tree adders into spacer phase.**
- **Providing simultaneous switching Booth encoder together with some part of the Wallace tree layers into spacer phase and executing complete work cycle by remaining Wallace tree layers.**

Dense FIFO: Control Unit



Conclusions

- **Development of the SI circuits is always a compromise between their performance and complexity. The necessity of an indication of all cells in the designed SI circuit significantly affects this compromise**
- **Three-stage pipeline implementation of SI multiplier provides 3 Gflops performance of the SI FMA**
- **Single-stage multiplier release provides the best "performance/complexity" ratio and the highest energy-efficiency**
- **Proposed few-stage SI FIFO on basis of SI dense shift register provides the best characteristics and higher energy-efficiency**

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