# FAULT-TOLERANCE OF THE SELF-TIMED CIRCUITS

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# INTRODUCTION

- The most frequently appeared logical faults in the CMOS circuits:
  - Short-term single transient event (SET), resulting in "false" pulses in the logical nets
  - Single event upset (SEU)
- Fault mitigation techniques:
  - Architectural and schematic redundancy
  - Noise resistant codes and fault-tolerant codes

# SELF-TIMED CIRCUITS

ST circuits are ideologically resisted to the most part of the short-term single failures due to their fundamental features:

- Redundant dual-rail and bi-phase signal coding
- Diphase functional discipline
- Indication of all switch completion

# SELF-TIMED CIRCUITS

- **Advantages of the ST circuits:**
  - Independence on cell's delays
  - Wide workability range on power supply and temperature
  - Localization of the constant faults
- **Penalties:**
  - Hardware redundancy
  - Increased signal number

# SELF-TIMED CIRCUITS

## ST dual-rail signal coding with null spacer

| X | XB | State |
|---|---|---|
| 0 | 0 | spacer |
| 0 | 1 | Bit “0” |
| 1 | 0 | Bit “1” |
| 1 | 1 | “anti-spacer” (illegal) |

**“Anti-spacer” may appear as a result of the soft fault**

# SELF-TIMED CIRCUITS

Solution: “anti-spacer” is indicated as second spacer (spacer1) to prevent malfunction

| X | XB | State |
|---|---|---|
| 0 | 0 | spacer0 |
| 0 | 1 | Bit “0” |
| 1 | 0 | Bit “1” |
| 1 | 1 | spacer1 |

# CRITICAL FAULTS IN COMBINATIONAL ST CIRCUITS

A. Switching of any dual-rail signal into anti-spacer state in work phase during work phase

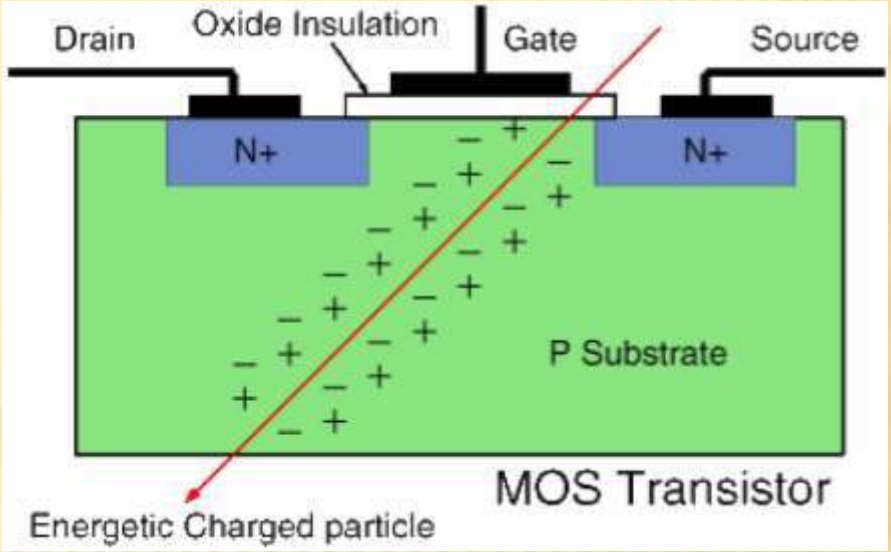
B. Switching of any dual-rail signal into inverse work state before spacer phase completion indication

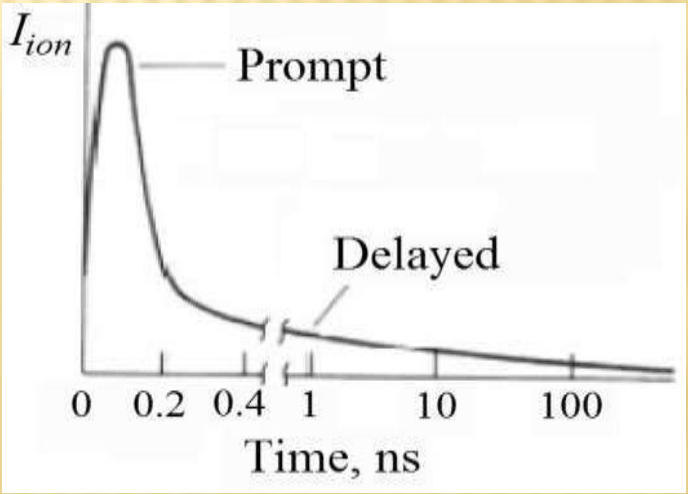
C. Switching of some dual-rail signal into any work state after spacer phase completion indication

# PHYSICAL REASONS OF THE SOFT FAULTS IN CMOS

- Cosmic rays
- Near-earth radiation
- Induced radiation

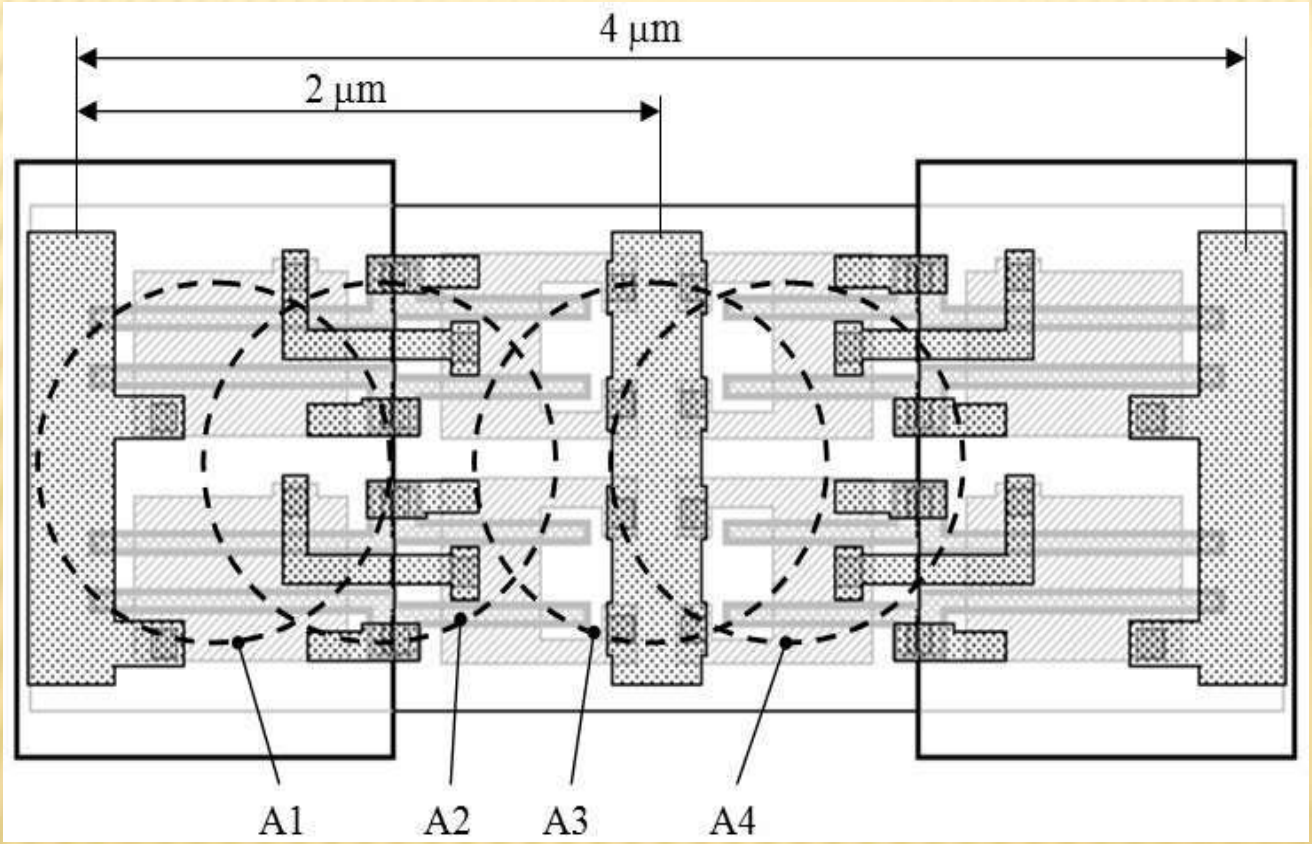
**Ionization current**



# REAL IMPACT IN 65-NM CMOS CIRCUITS

Effective diameters of heavy charged particle's track in 65-nm CMOS standard cell layout (four adjacent NAND2 gates)

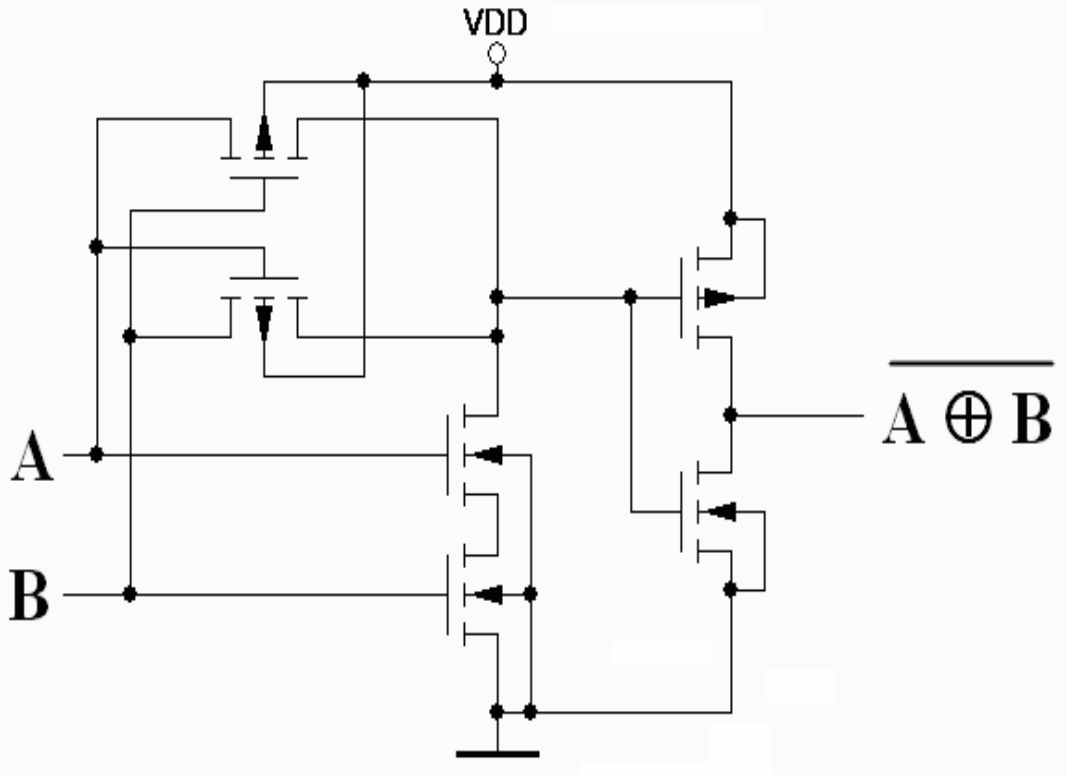



Ionization current have the same direction in impacted gates

Work state that is opposite to the expected one is impossible

# INDICATION OF THE DUAL SPACER

Usage of a monotonic “exclusive OR” cell without an inverted inputs




6 CMOS transistors instead of four ones in the indication cell

# FAULT-TOLERANCE OF THE COMBINATIONAL ST CIRCUITS

- **Dual-rail coding**
- **Diphase functional discipline**
- Dual spacer
- Completion indication

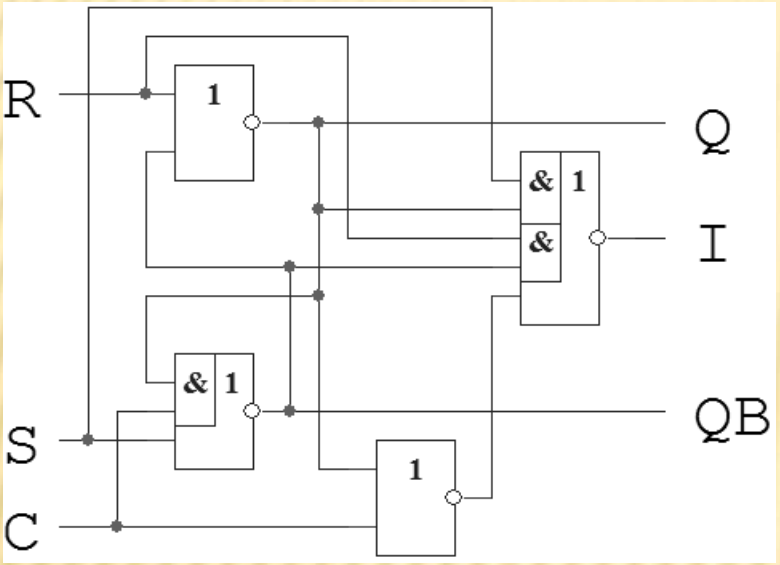
Combinational ST circuits are immuned to 82% of all soft faults

# ST TRIGGER'S FEATURES

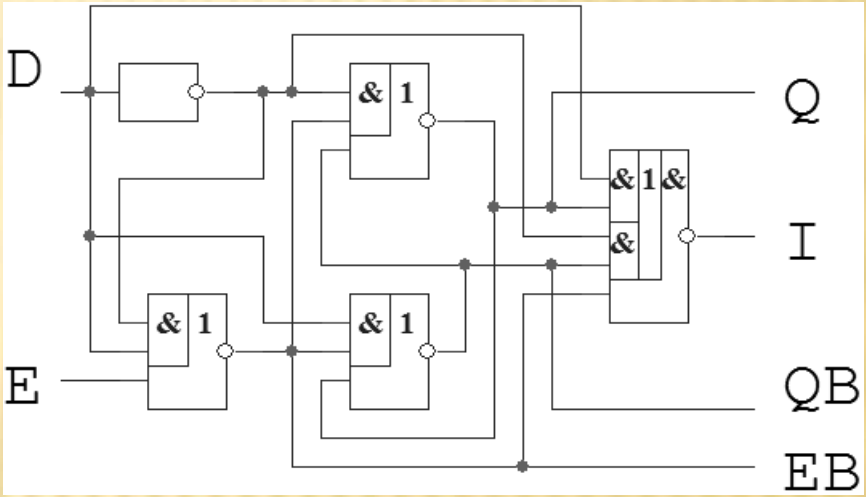
- **Schematic Basis: bistable cell (RS-trigger)**
- **Diphase functional discipline plus transit state**
- Bi-phase and dual-rail coding
- Completion indication (outputs-to-inputs correspondence in both work phases)

# ST TRIGGER EXAMPLES: LATCHES

## RS-Latch

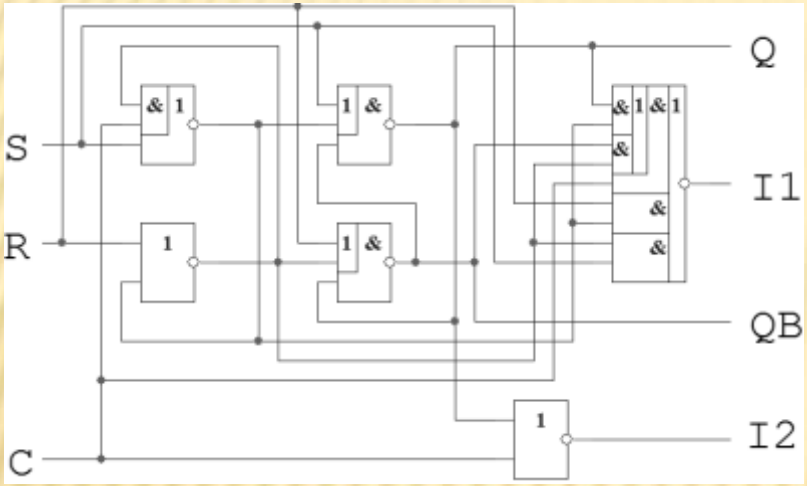



## D-Latch

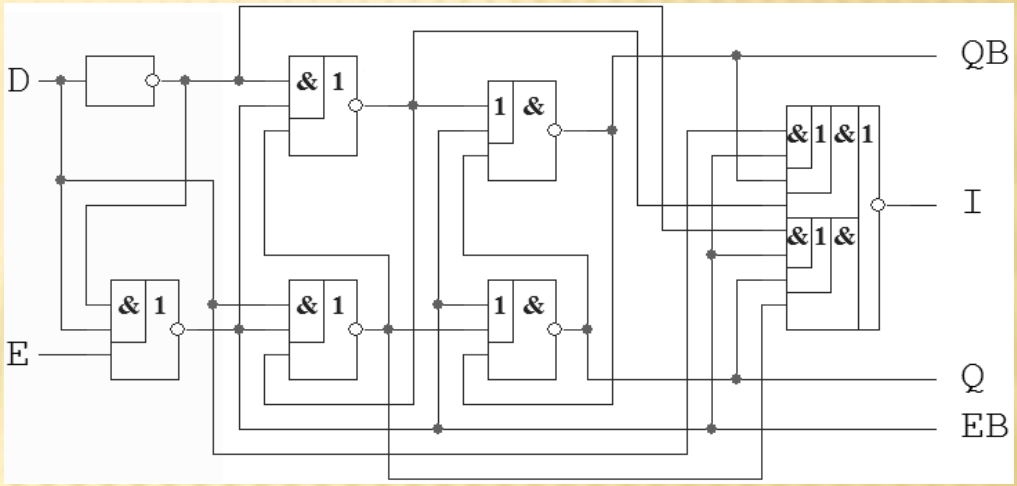


# ST TRIGGER EXAMPLES: FLIP-FLOPS

## RS-Flip-flop




## D-Flip-flop

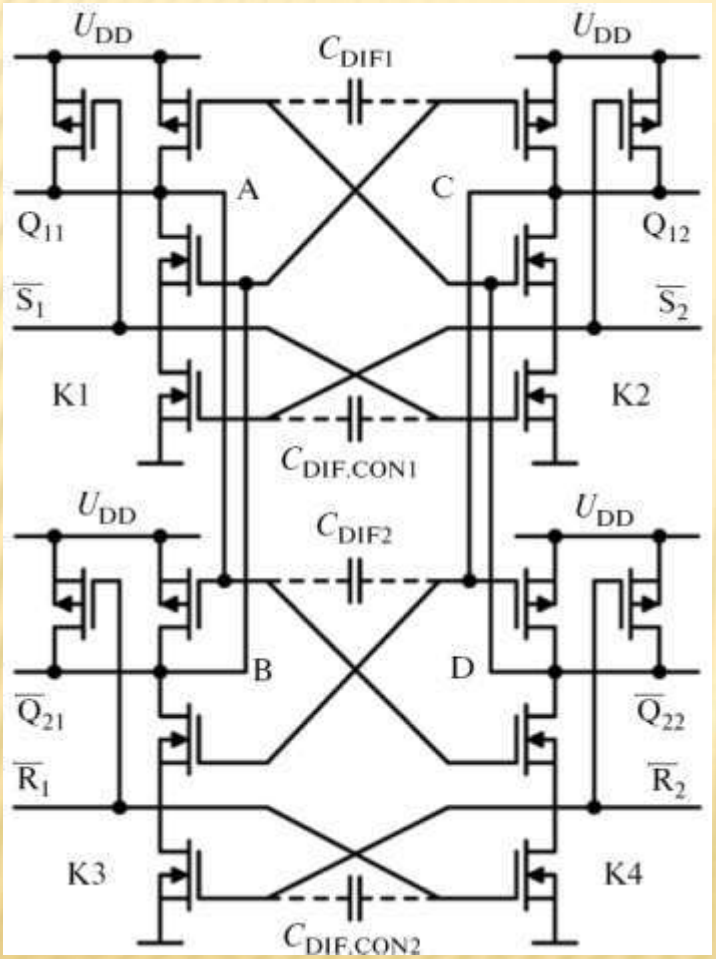


# CRITICAL FAULTS IN ST TRIGGERS

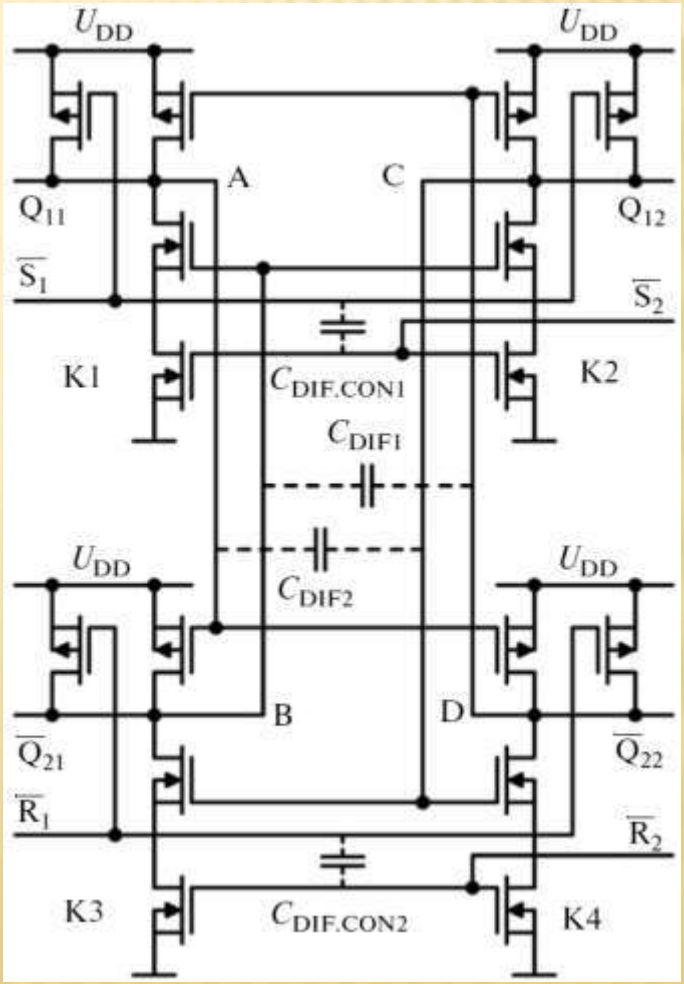
- Switching output to an opposite state before trigger's indicator transients into a work value
- Switching indicator to a value that doesn't match the current phase
- Appearance of the "anti-transit" state at the outputs in work or spacer phase etheir before or after switching trigger's indicator to corresponding value
- Switching first bistable cell to an opposite state at its spacer phase etheir before or after appearing spacer value at the trigger's indication output
- Premature indication output switching to a value corresponding to the current phase

# SCHEMATIC ENHANCEMENTS

## DICE technique




## Quatro technique



# FAULT-TOLERANCE OF ST TRIGGERS

- Bi-phase and dual-rail coding
- Diphase functional discipline
- Outputs-to-inputs correspondence indication
- DICE & Quatro implementation

ST triggers are immuned to 80% of all soft faults

# CONCLUSIONS

- Up to 82% of all soft faults in combinational ST circuits and up to 44% of all soft faults in ST triggers are masked due to hardware redundancy and completion indication
- The usage of the DICE-like or Quatro-like approach for implementing ST triggers at schematic and layout level will additionally increase the ST trigger's fault-tolerance up to 80%
- Our following study will be devoted to usage of a ternary logic for advancing fault-tolerance of the self-timed circuits

# Thanks!

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