SPEED-INDEPENDENT FLOATING POINT COPROCESSOR

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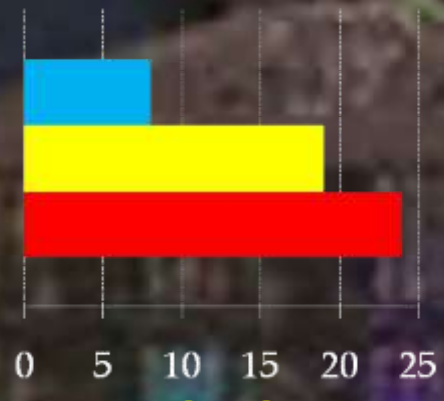
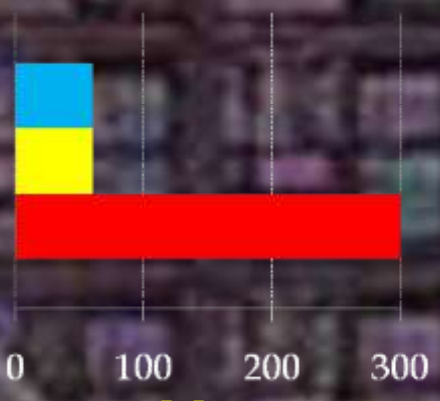
Why Speed-Independent circuits?

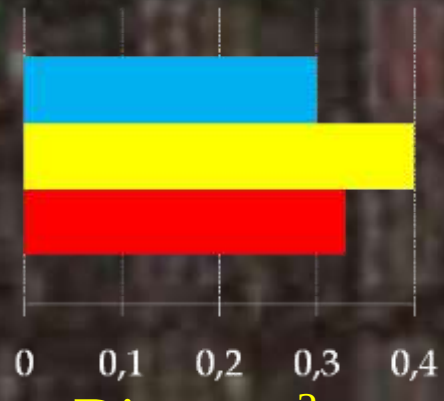
- They reduce power consumption due to removing both clock generator, and "clock tree" out of a circuit
- They have wide workability range on power supply and temperature

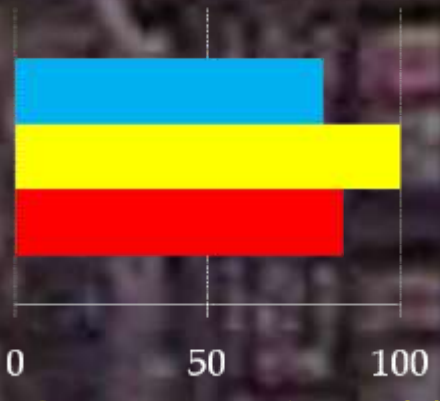
Divider & Square Rooter, 0.18µ



Parameter	Variant		
	■	■	■
Maximum performance at any environment	√	–	–
Extended workability range	√	–	–
Constant faults detection	√	–	–
Average power consumption	√	–	√
Minimum noise level	√	–	–

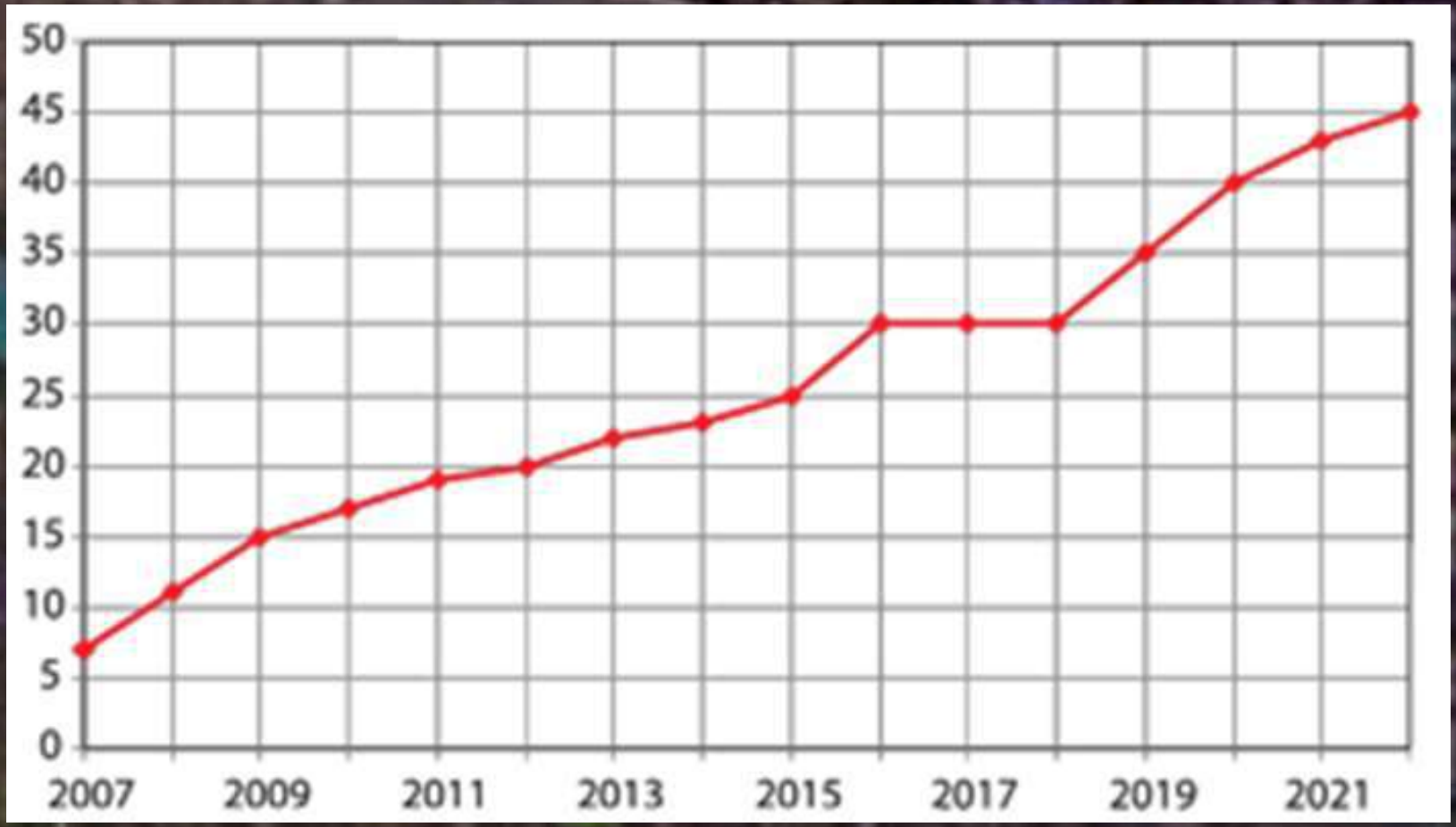




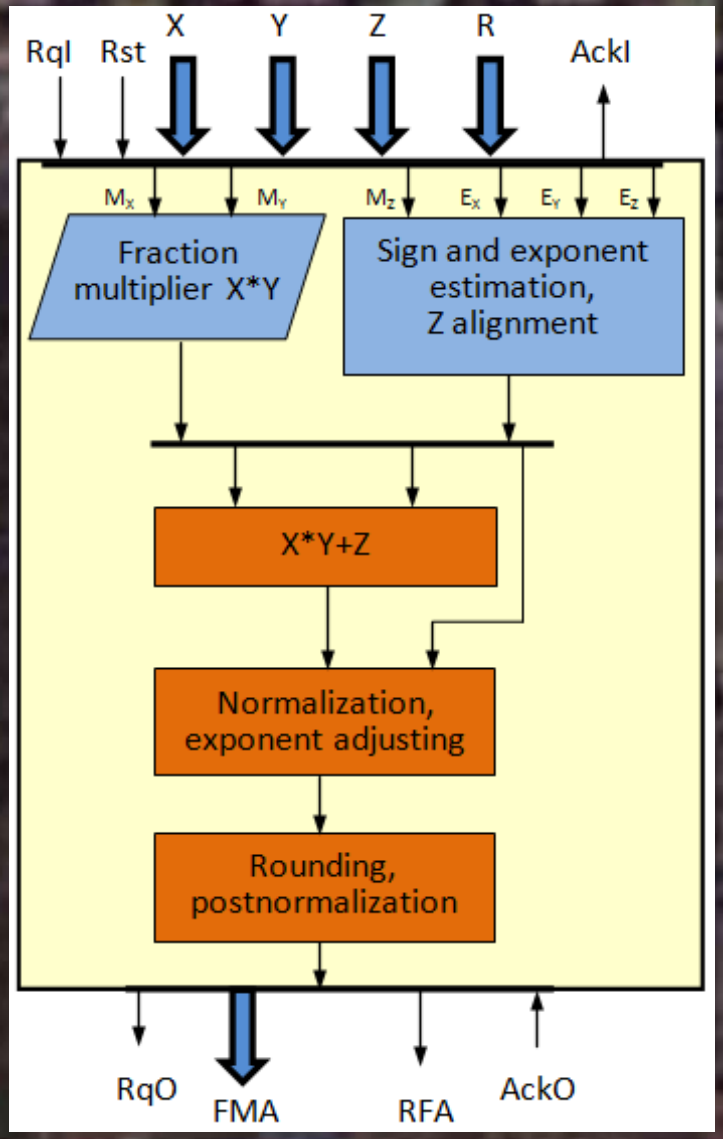


■ Synchron, "SRT-4" ■ Synchron, "Newton" ■ Quasi-SI, "SRT-2"

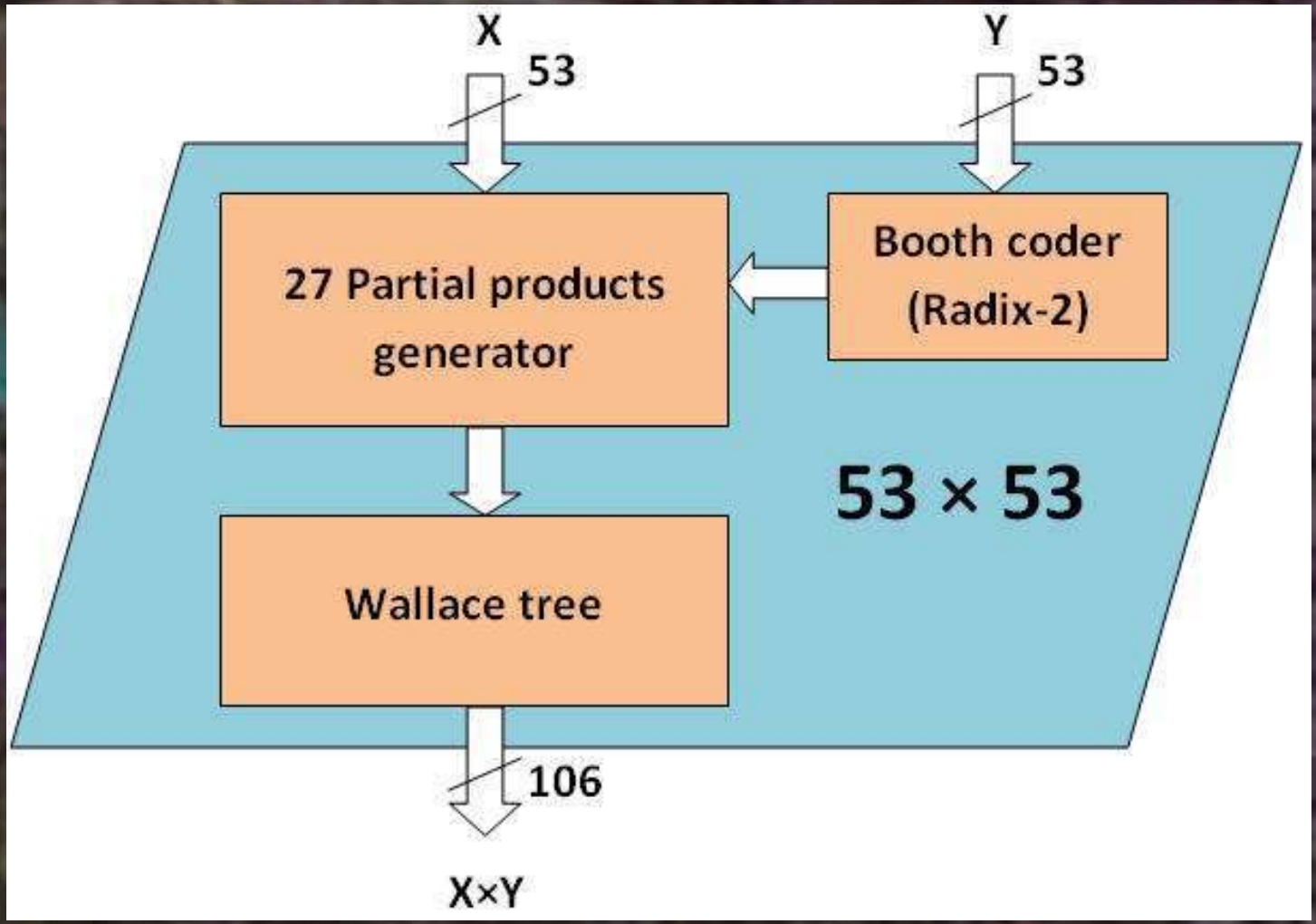
Projected part of SI-logic (ITRS)



Structure chart of SI-FPC



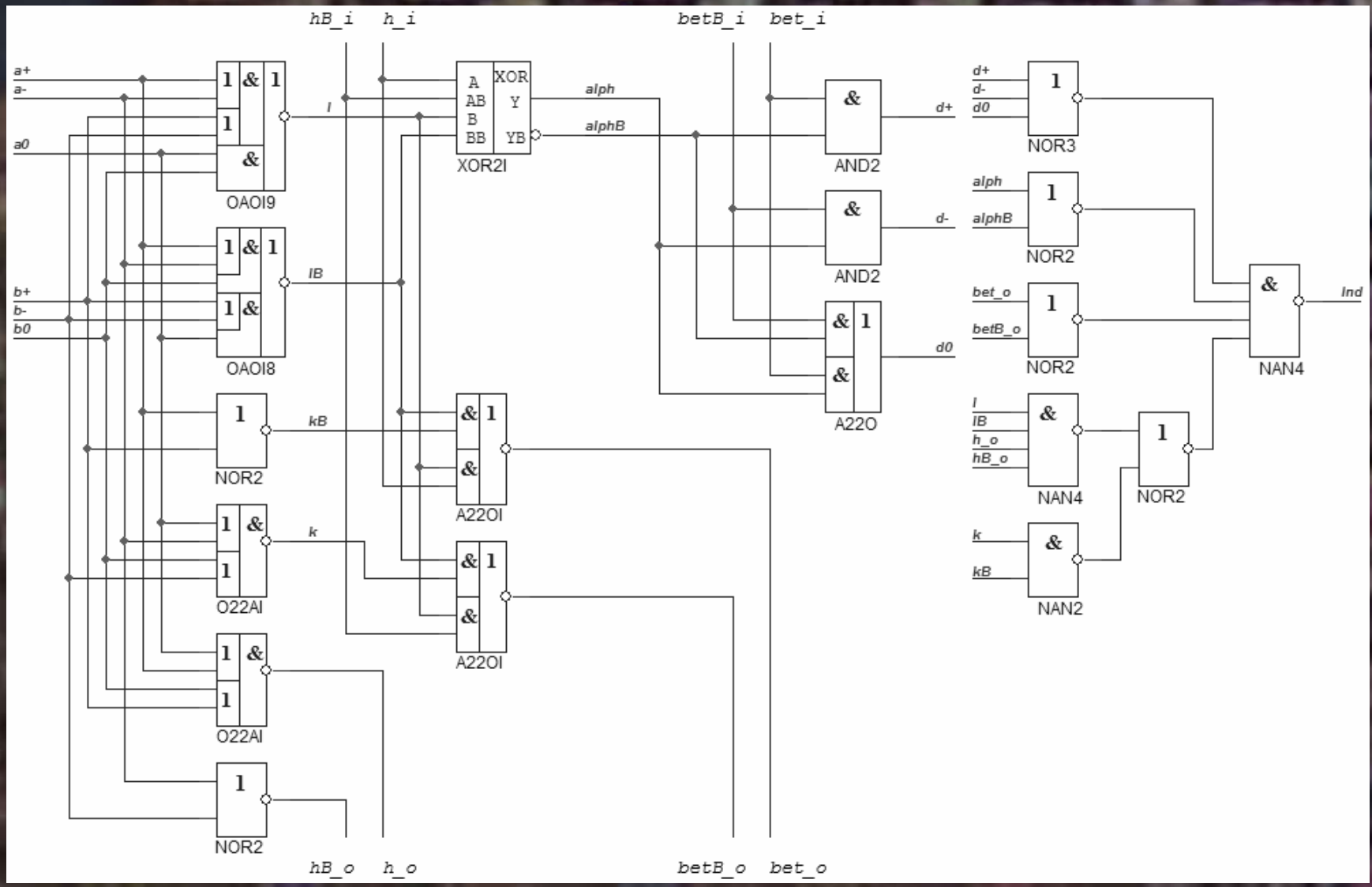
Booth multiplier



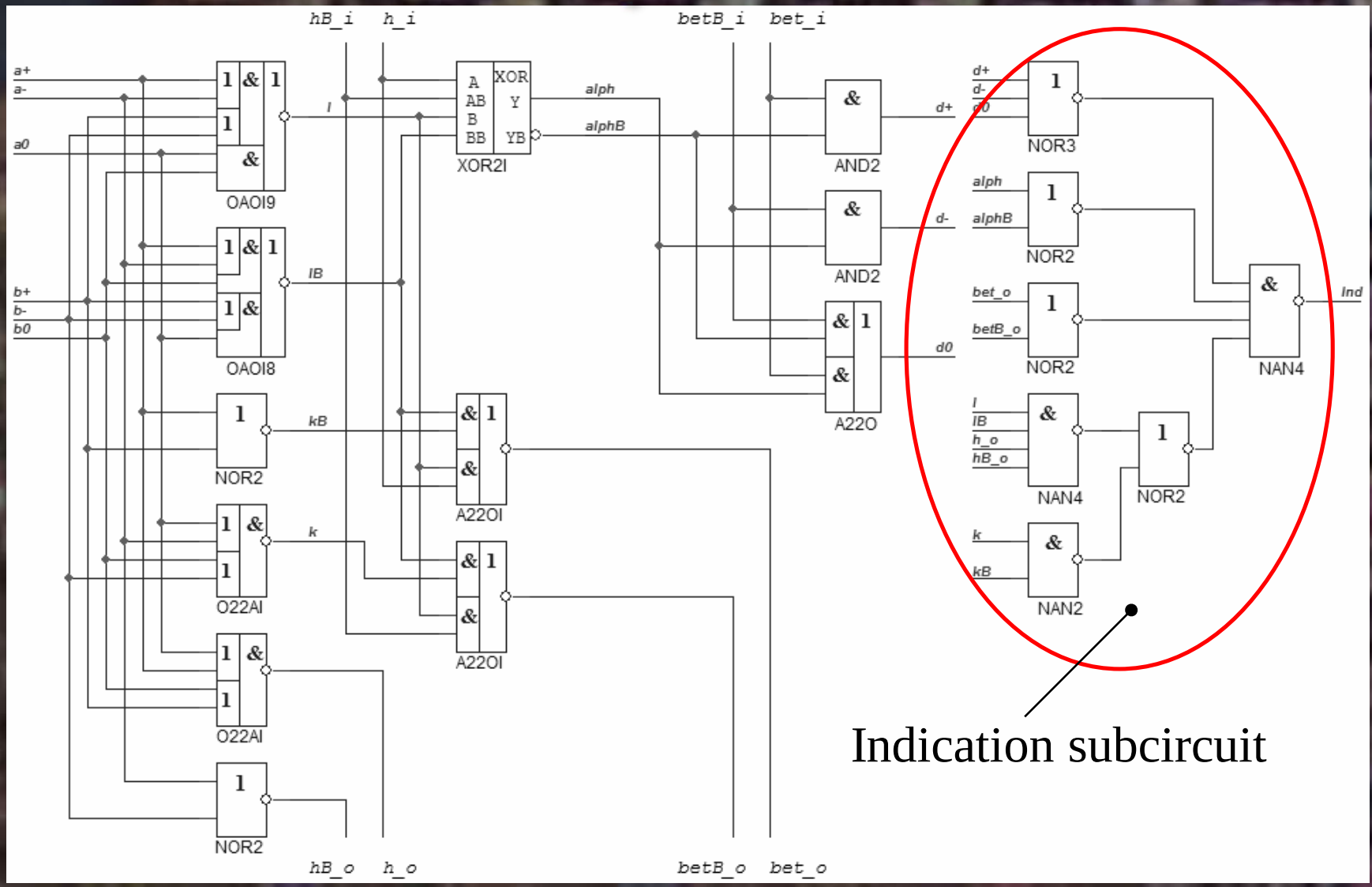
Ternary ST-coding

Synchronous redundant code			Self-Timed redundant (ternary) code			
State	Binary code		State	ST ternary code		
	A	B		Ap	Am	An
+1	1	0	+1	1	0	0
0	0	0	0	0	0	1
–1	0	1	–1	0	1	0
N/A	1	1	spacer	0	0	0

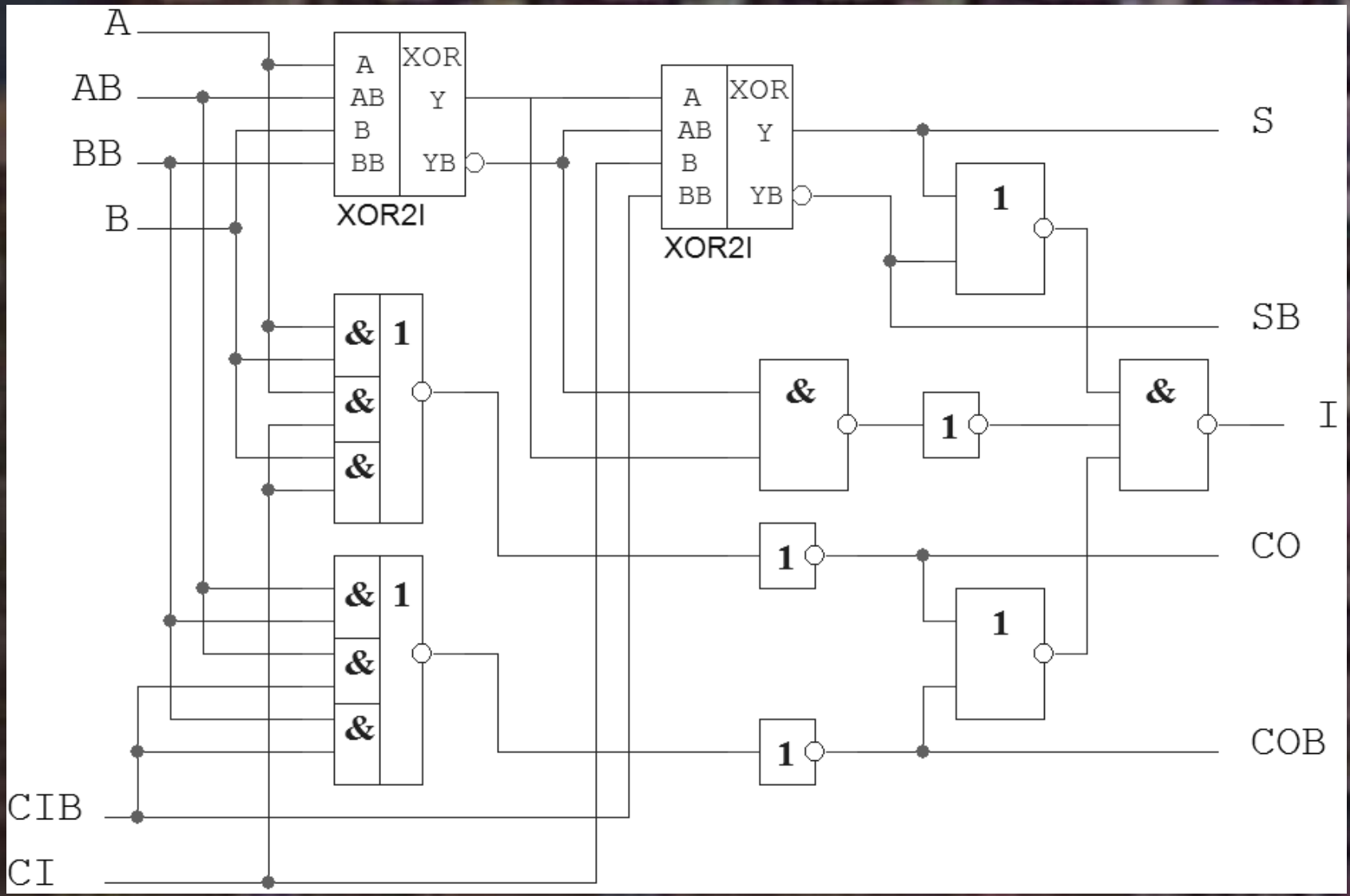
Ternary SI-adder



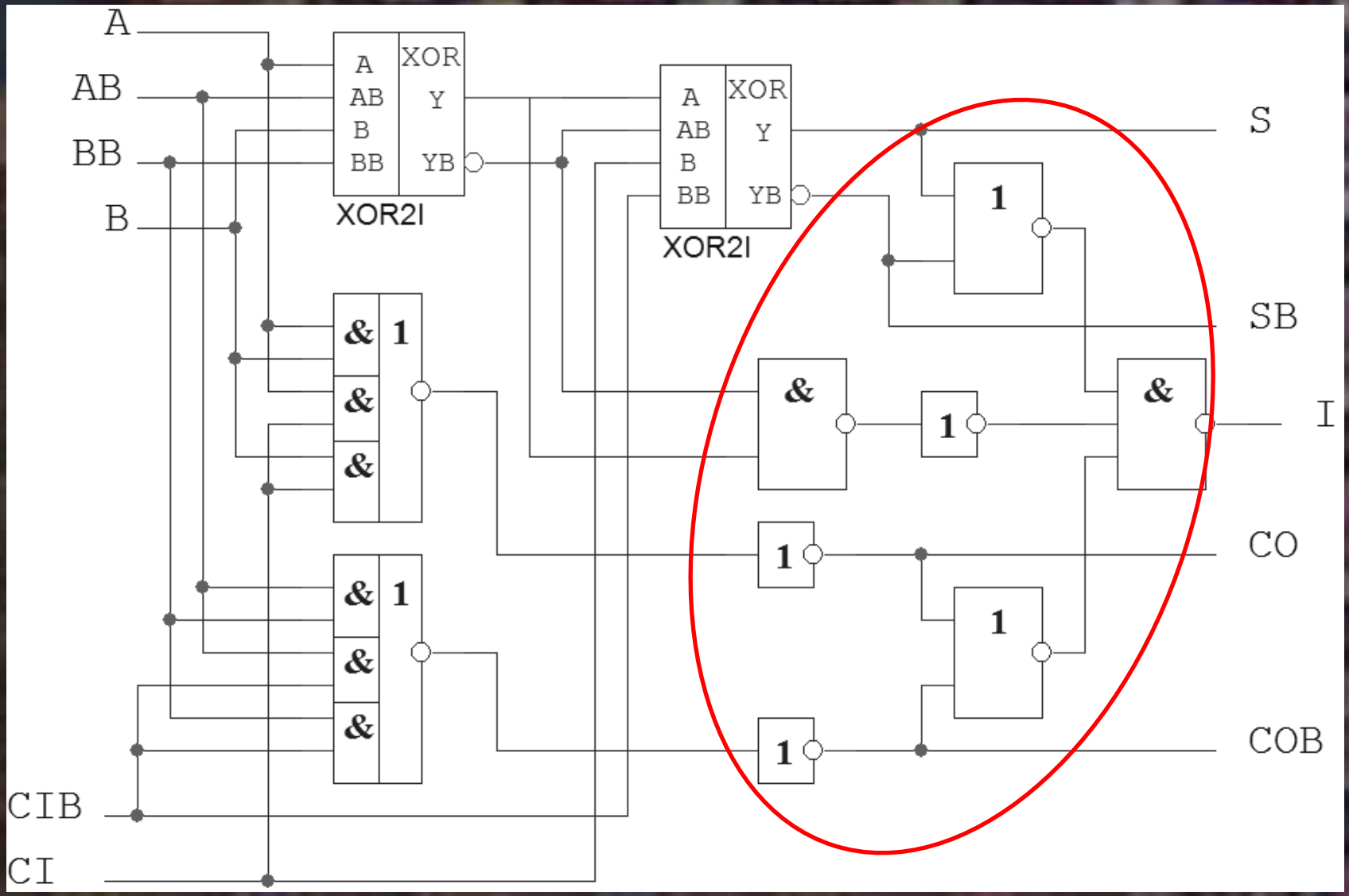
Ternary SI-adder



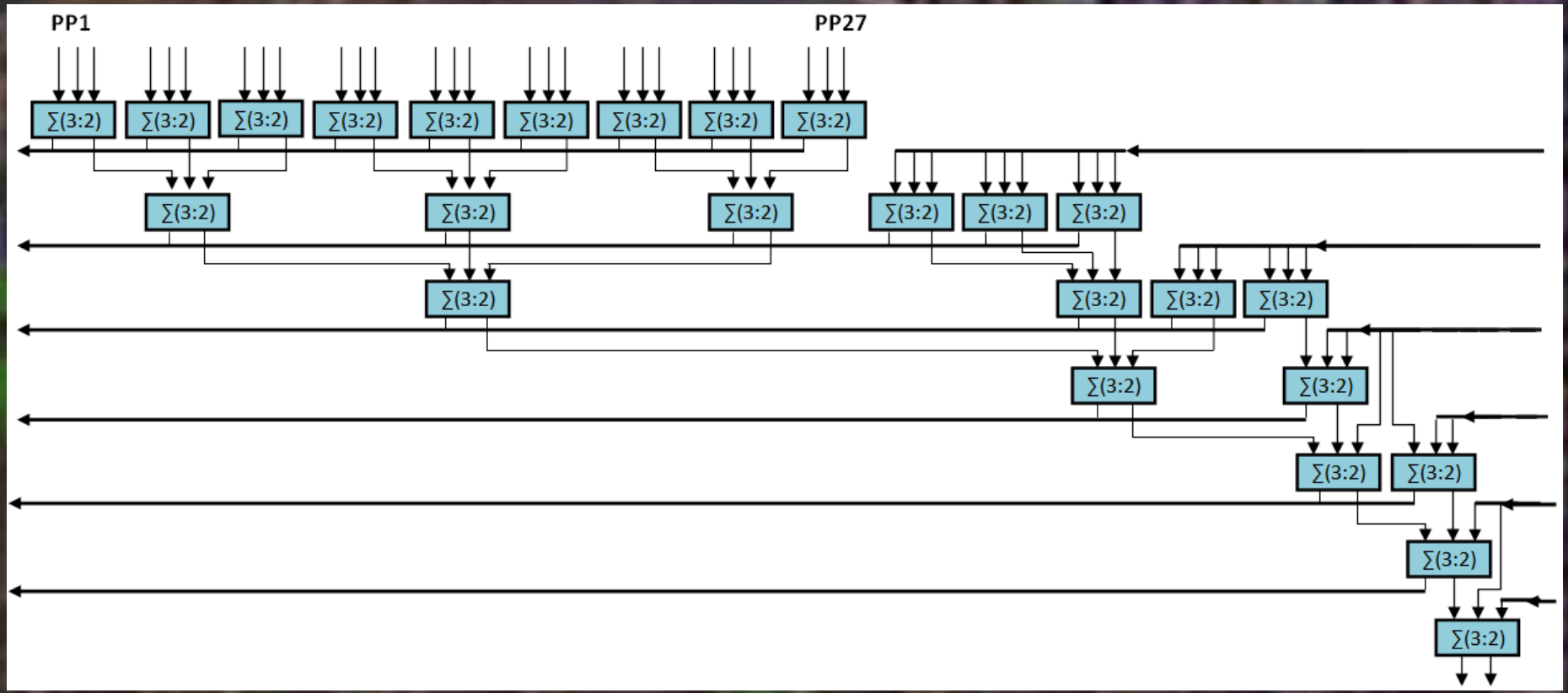
Dual-rail SI-adder



Dual-rail SI-adder

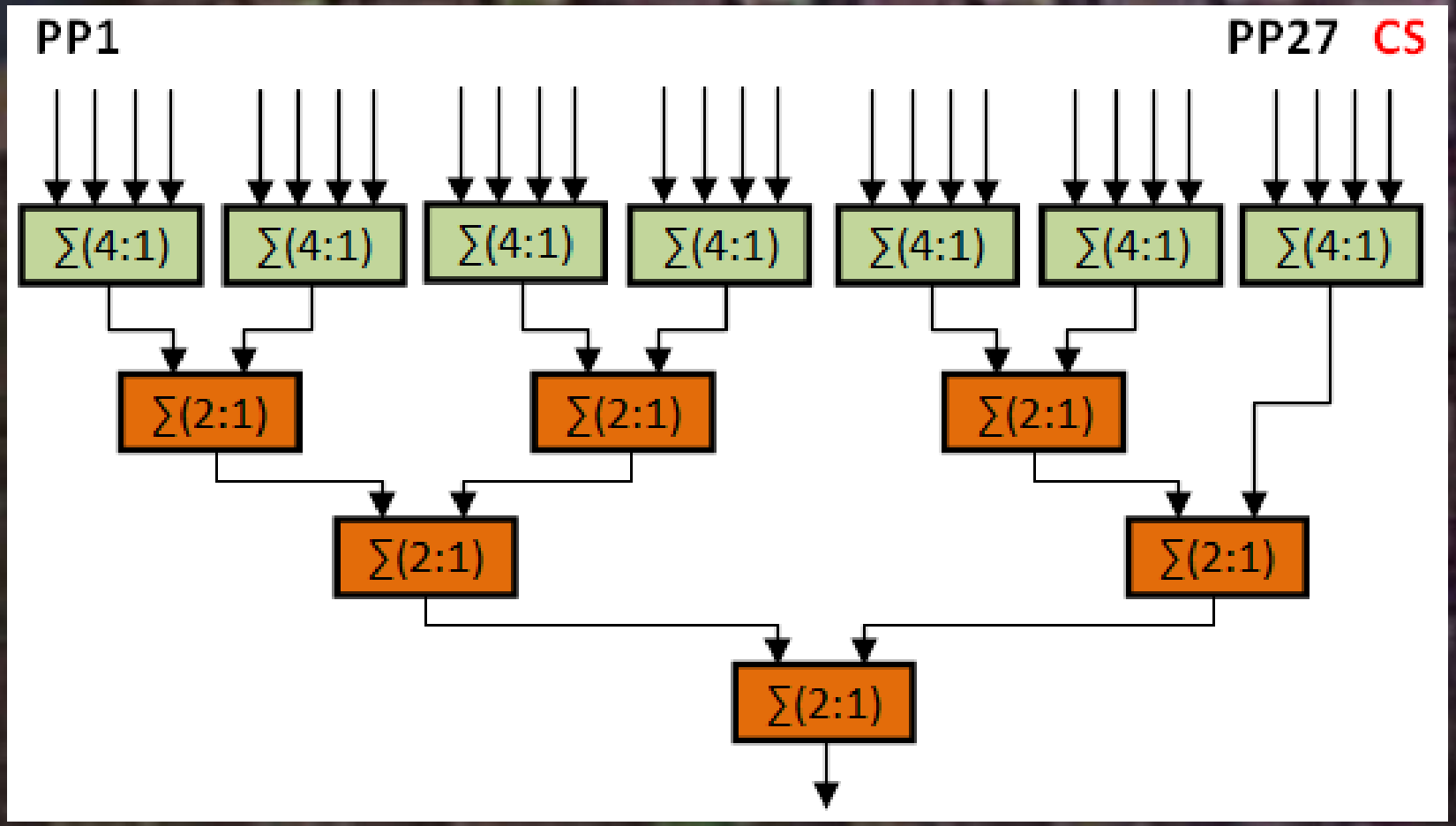


Dual-rail Wallace tree



1700 transistors, 7 stages

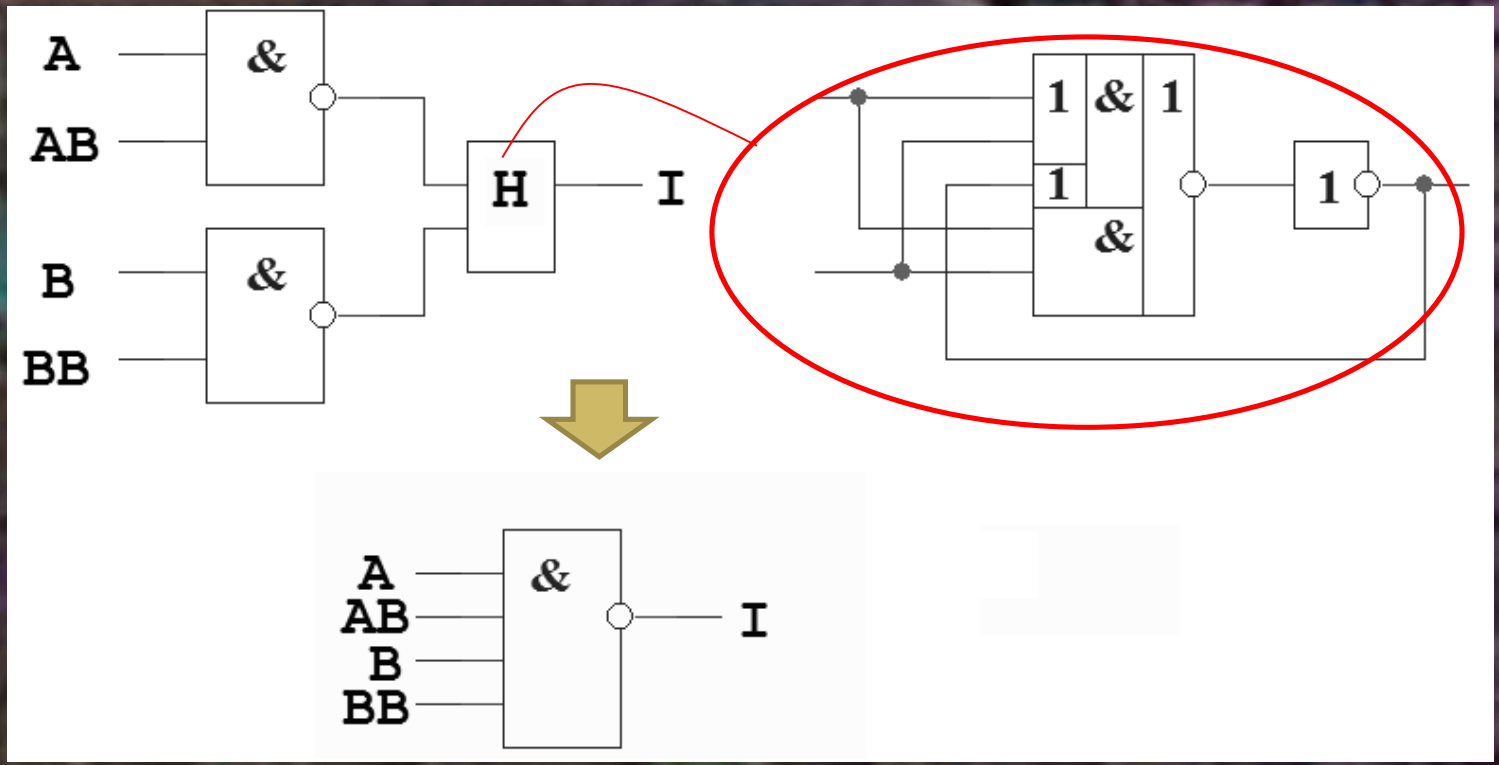
Ternary Wallace tree



2190 transistors, 4 stages

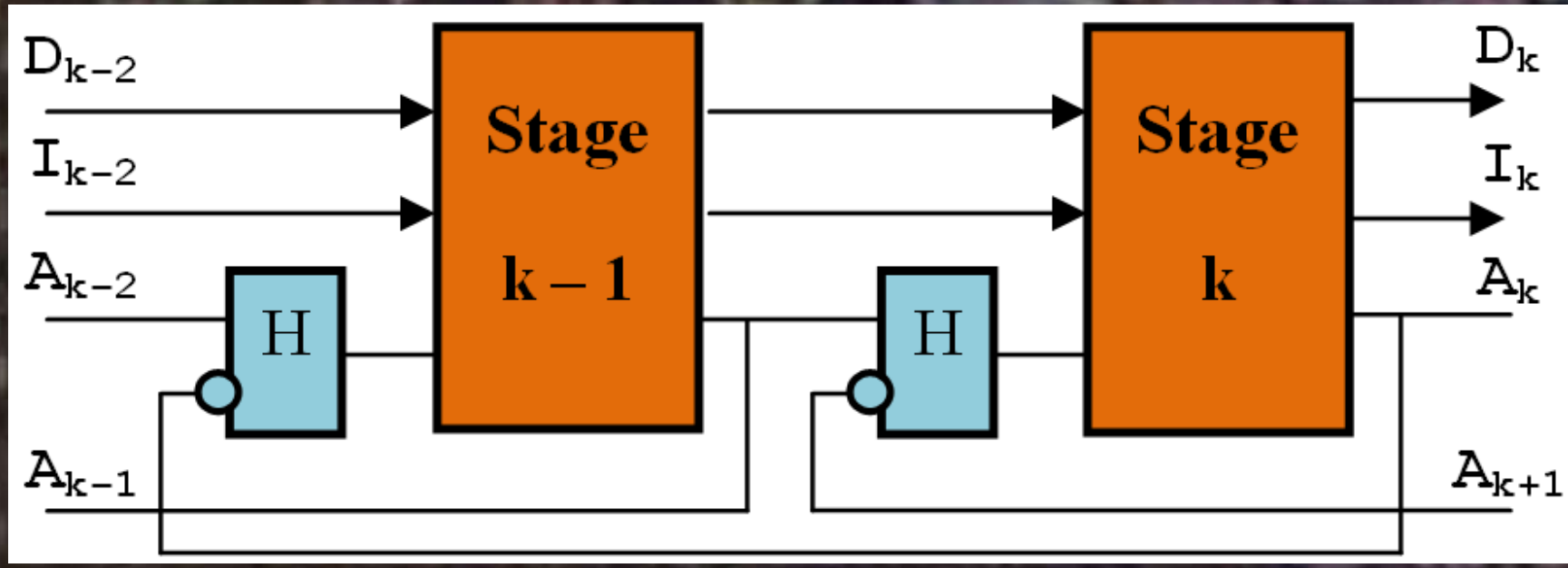
Simplified indication

- Full indication only in spacer phase

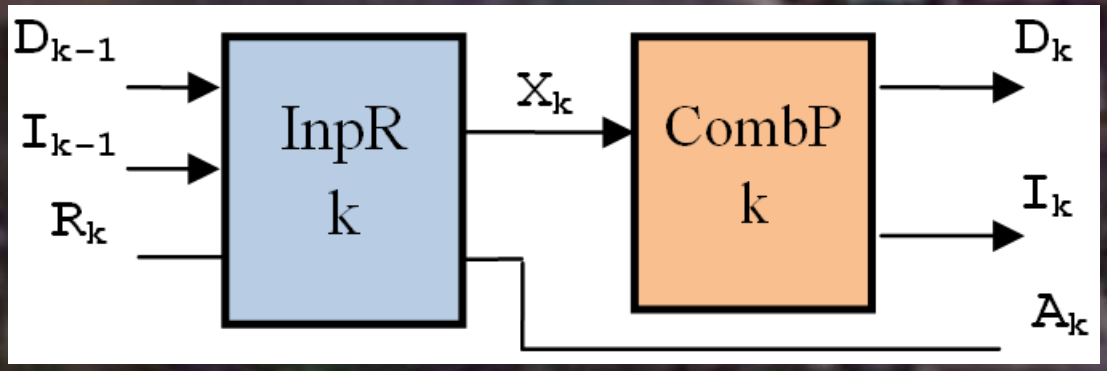


- Bitwise indicators

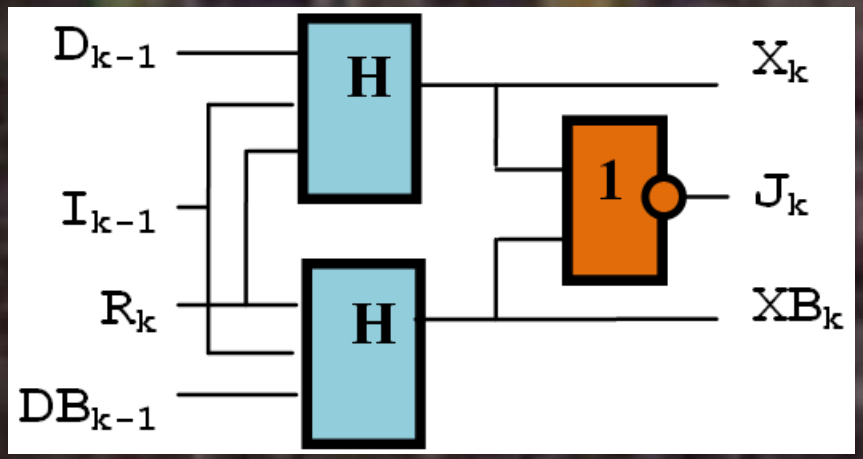
Pipeline organization: Top view



Pipeline organization: One stage



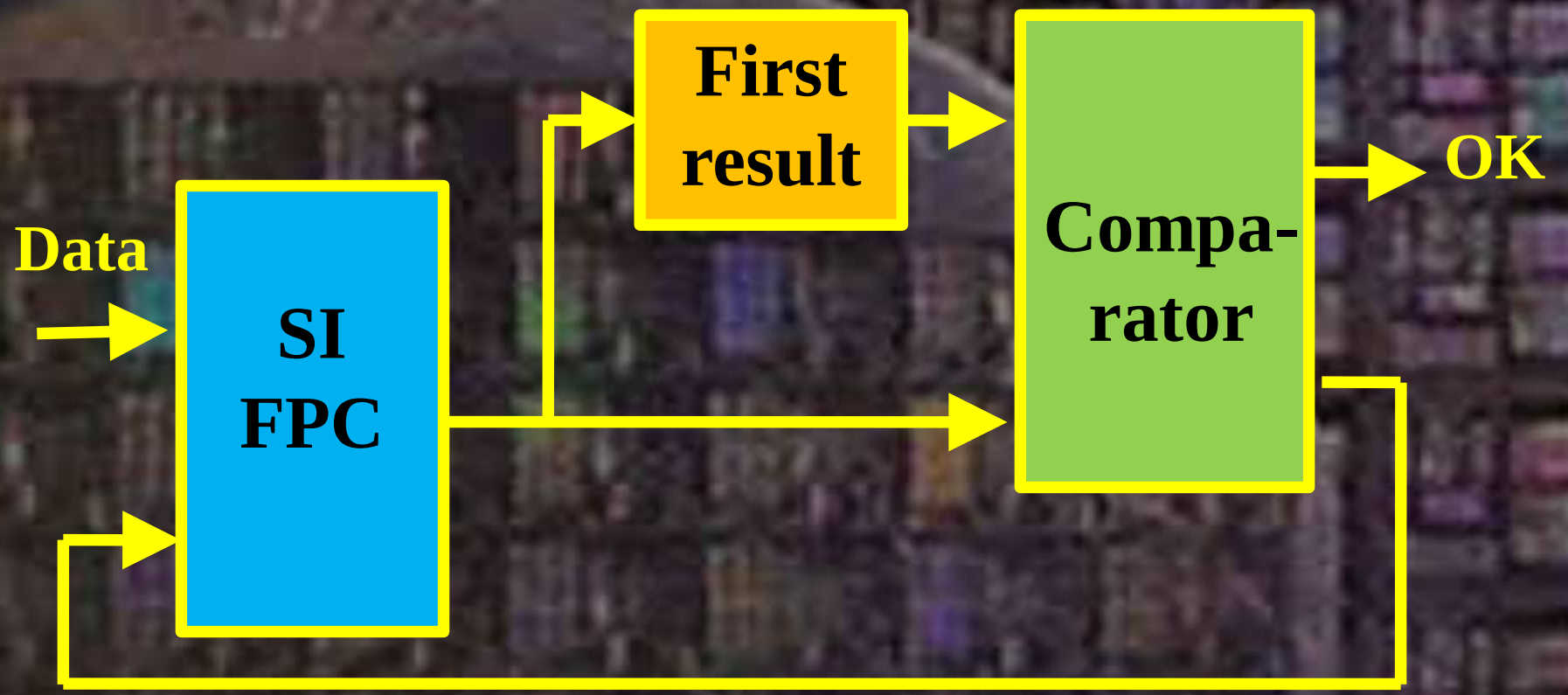
One bit of input register InpR



SI FPC's parameters

Parameter	Value
Complexity, transistors	315 000
Die size, mm^2	0.47
Performance, Gflops	0.54
Latency, ns	1.9
Power consumption, mW/Gflops	450

Testing SI-Coprocessor



Conclusions

- At first time in the world, really SI-FPC unit performing FMA operation was implemented
- Usage of ternary ST-code provided best performance of the Wallace tree
- Simplified indication allowed for reducing both the complexity and work phase time
- Two-stage pipeline sufficiently decreased hardware cost at minimal drop of performance

Thanks!

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