FUNCTIONAL APPROACH IN SELF-TIMED CIRCUIT DESIGN

Plekhanov Leonid, Zakharov Victor,
Stepchenkov Yuri

Institute of Informatics Problems, Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences, IPI RAS, Moscow, Russian Federation

Contents

- Event-driven analysis of SI-circuits
- Functional analysis of SI-circuits:
  - Low level analysis
  - High level analysis
- Synthesis of SI-circuits
- Conclusions

Essence of event-driven analysis

Analyzed circuit should be presented in a closed feed-back form:

only outp backs

Problems of event-driven analysis

- Analysis is carried out only for one initial state – completeness is far of practical needs
- Exponential dependence of the computational complexity on the number of elements and degree of parallelism

Event-driven analysis: Change Diagrams, part 1

Circuit	Micro-pipeline control queue		Asynchronous switch	
CAD Tool	Time, sec	Memory / disk swaping	Time, sec	Memory
TRANAL	180	400 Kbytes /+	0.28	100 Kbytes
VERDECT	300	22 Mbytes /-	0.99	122 Kbytes
TRASPEC	1	100 Kbytes /-	0.38	100 Kbytes

Event-driven analysis: Change Diagrams, part 2

CAD tools	Paral-lelism	Circuit level	Memory for state, Gbyte	Number of states per hour, 10^6
TRANAL	5-6	cells	0.64	0.3
BTRAN	12-16	modules	2	1.0
ASYAN	18 -24	blocks	48	200

Event-driven analysis: software tools from IPI RAS

Unit's type – capacity / parallelism	Analysis time, min*)		
	BTRAN	ASYAN	ASPECT
Binary counter – 4 / 1	0.01	0.12	0.02
Shift register – 4 / 4	0.21	0.97	0.02
Microcore – 4 / 47	–	0.53	0.02
ALU – 64 / 293	–	–	0.14
Divider – 16 / 330	–	–	1588
Divider – 64 / 1024	–	–	27360

*) for single state of inputs and triggers

Functional approach

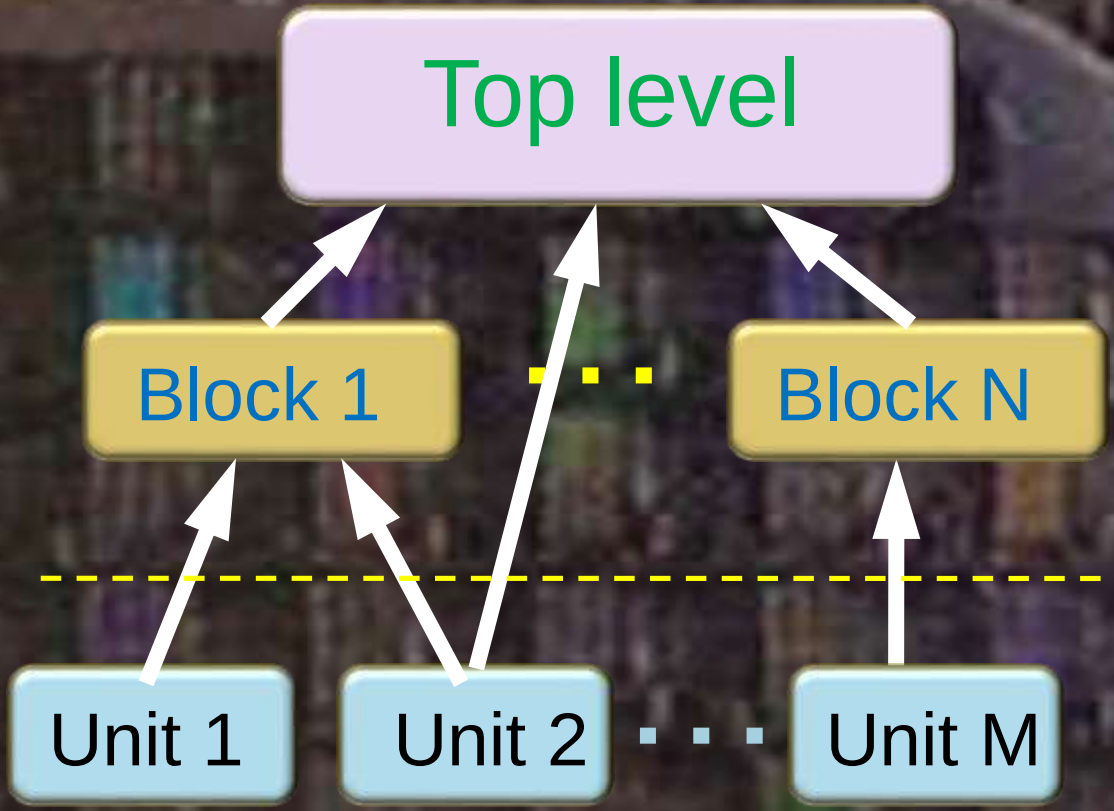
- Analyzes the equations of circuits
- Deals with the open circuits
- Takes into account a nature of speed-independent circuits:
  - ST-coding of data
  - Two-phase operation discipline (work phase and spacer one)
  - Signal indication, and so on

Functional approach: SI circuit definition

An open circuit possessing two features:

- **Absence of races for any finite delay of the elements**
- **Indicativeness of all inputs, outputs and internal signals**

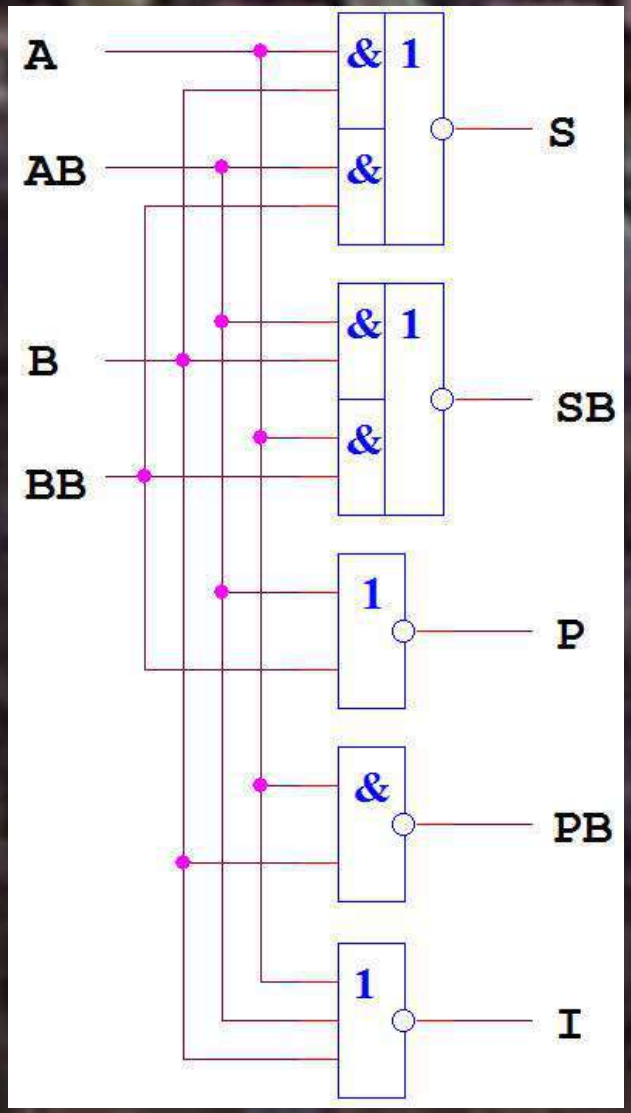
Functional approach: hierarchical analysis



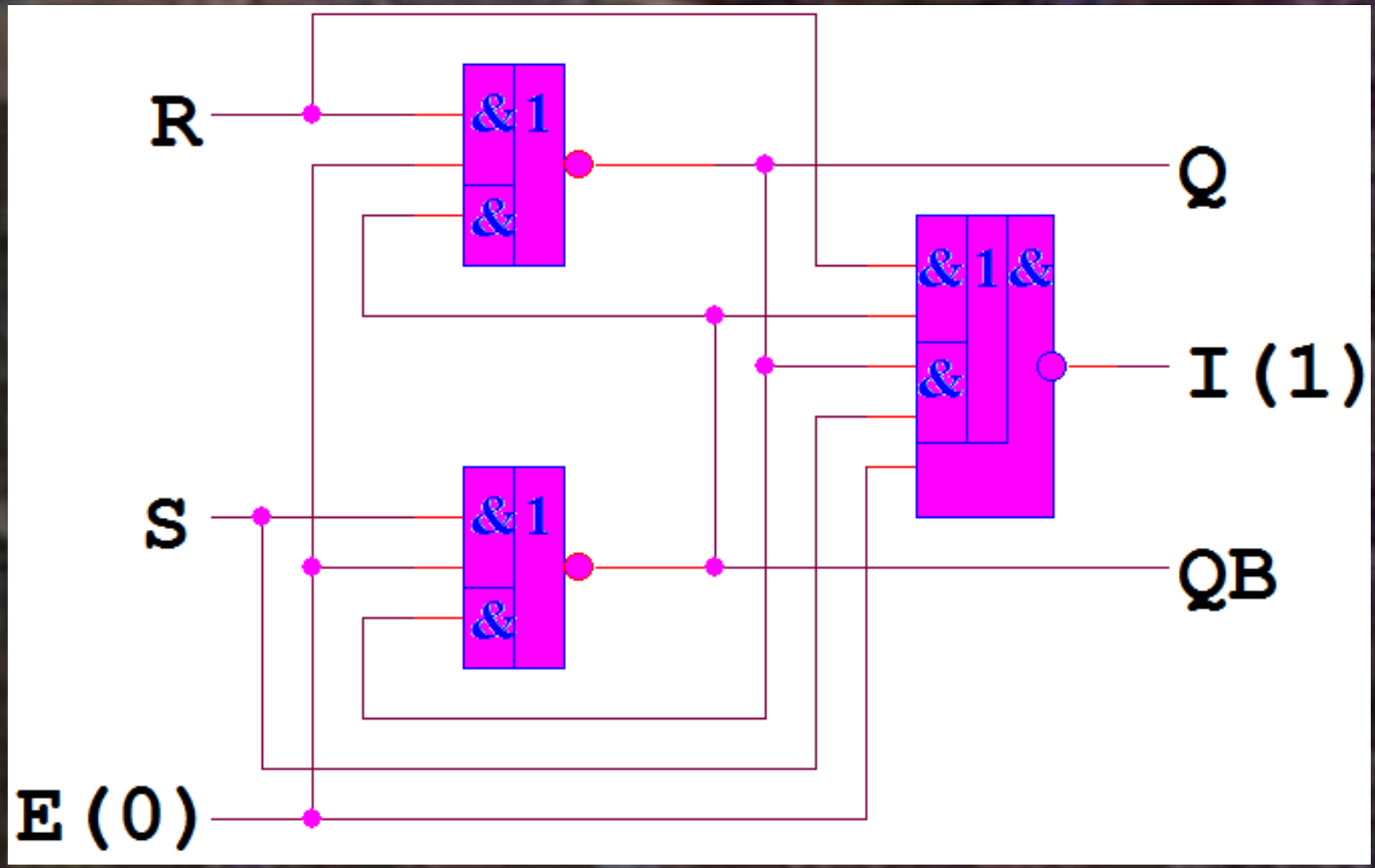
High levels: structural description

Lower level: logical function description

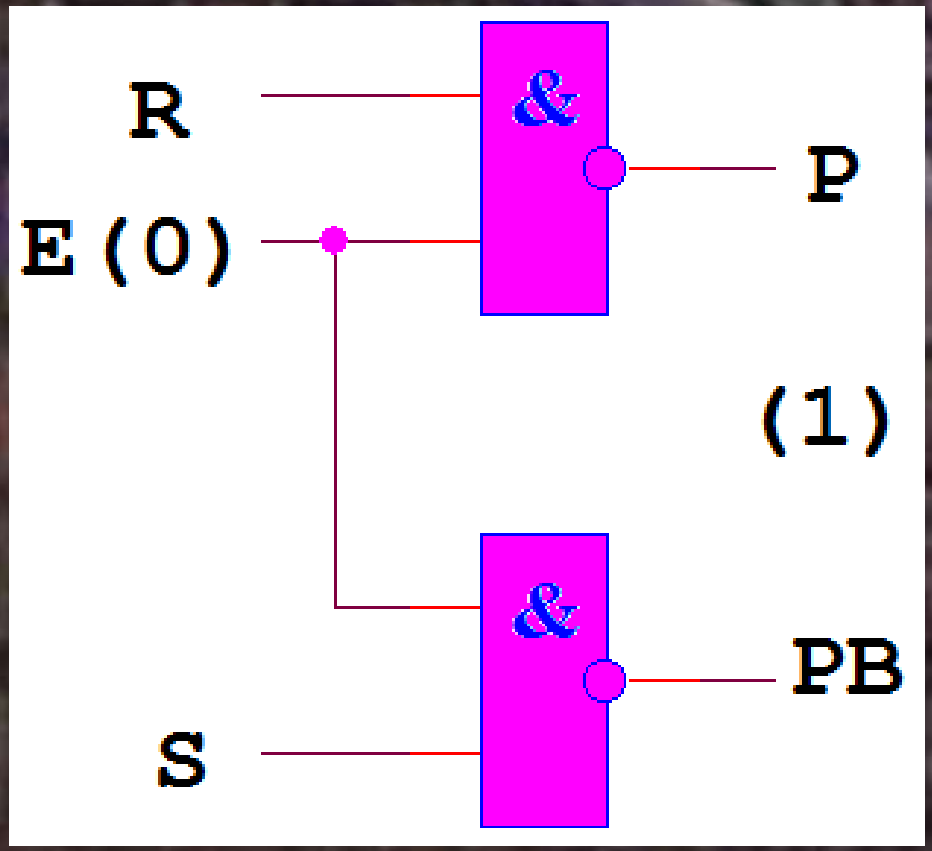
Low level analysis



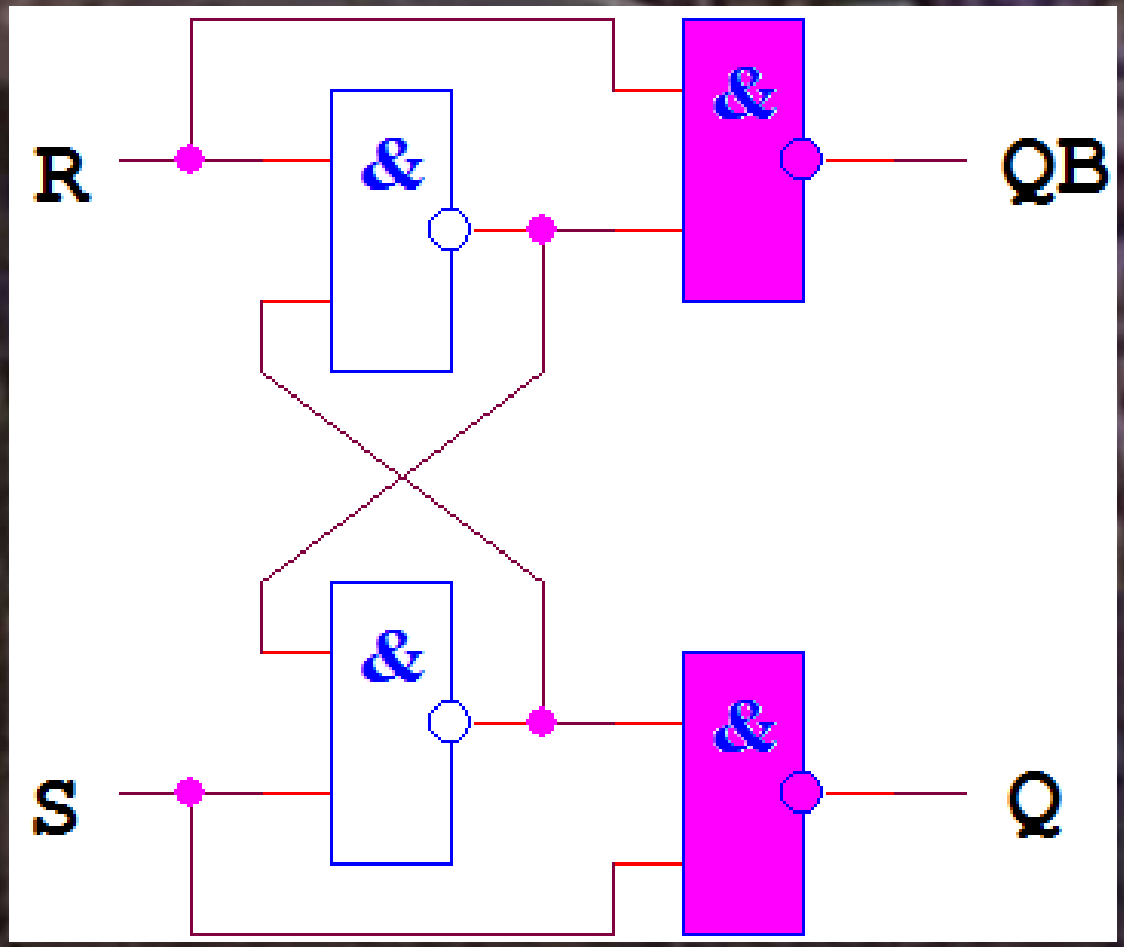
Low level analysis: races control



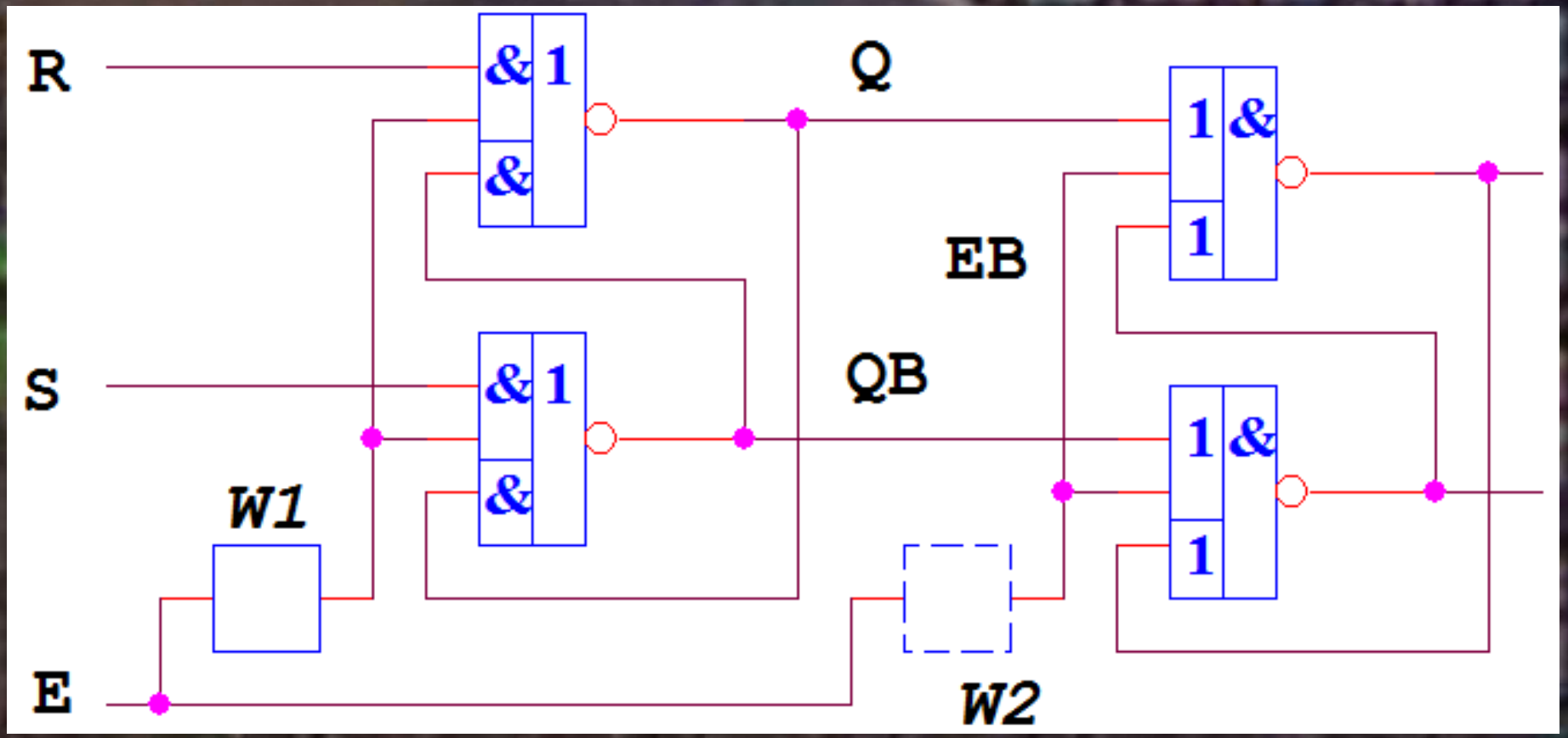
Low level analysis: races control



Low level analysis: races control



Low level analysis: connection control



High level analysis: checking lists & attributes

- Hierarhical approach on base of verified low level units
- Verifying connections
- Verifying indicativeness
- Verifying absence of races
- Preparing descriptions for next analysis level

Functional analysis via Event-driven analysis

Unit's type – capacity / parallelism	Analysis time, min	
	ASPECT*)	FAZAN
Microcore – 4 / 47	0.02	0.01

*) for single state of inputs and triggers

Synthesis of SI circuits

- Based on logical functions that are not self-timed
- Balanced by performance and complexity
- Minimized indication circuit
- Software tools

Synthesis of SI circuits

$F1 = A \wedge B,\ F2 = B \wedge C$

$V1 = A \wedge B,\ V2 = B \wedge C,$

$VB1 = AB \vee BB,\ VB2 = BB \vee CB,$

indications

$I1 = A \vee AB,\ I2 = B \vee C \vee BB \wedge CB$

Conclusions

- The functional approach provides the following advantages:
  - Analysis of SI-feature of open circuits
  - Hierarchical SI-analysis of VLSI and SoC
  - Synthesis of combinational circuits with dual-rail signals by given criterion of performance or complexity

Thanks!

Contacts

- Director: academician Sokolov I.A.
- Address: Institute of Informatics Problems of the Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences (IPI RAS), Moscow, Russian Federation, 119333, Vavilova str., 44, b.2
- Tel: +7 (495) 137 34 94
- Fax: +7 (495) 930 45 05
- E-mail: ISokolov@ipiran.ru

- Stepchenkov Y.A., tel. +7 (495) 671 15 20, Ystepchenkov@ipiran.ru