ADVANCED INDICATION OF THE SELF-TIMED CIRCUITS

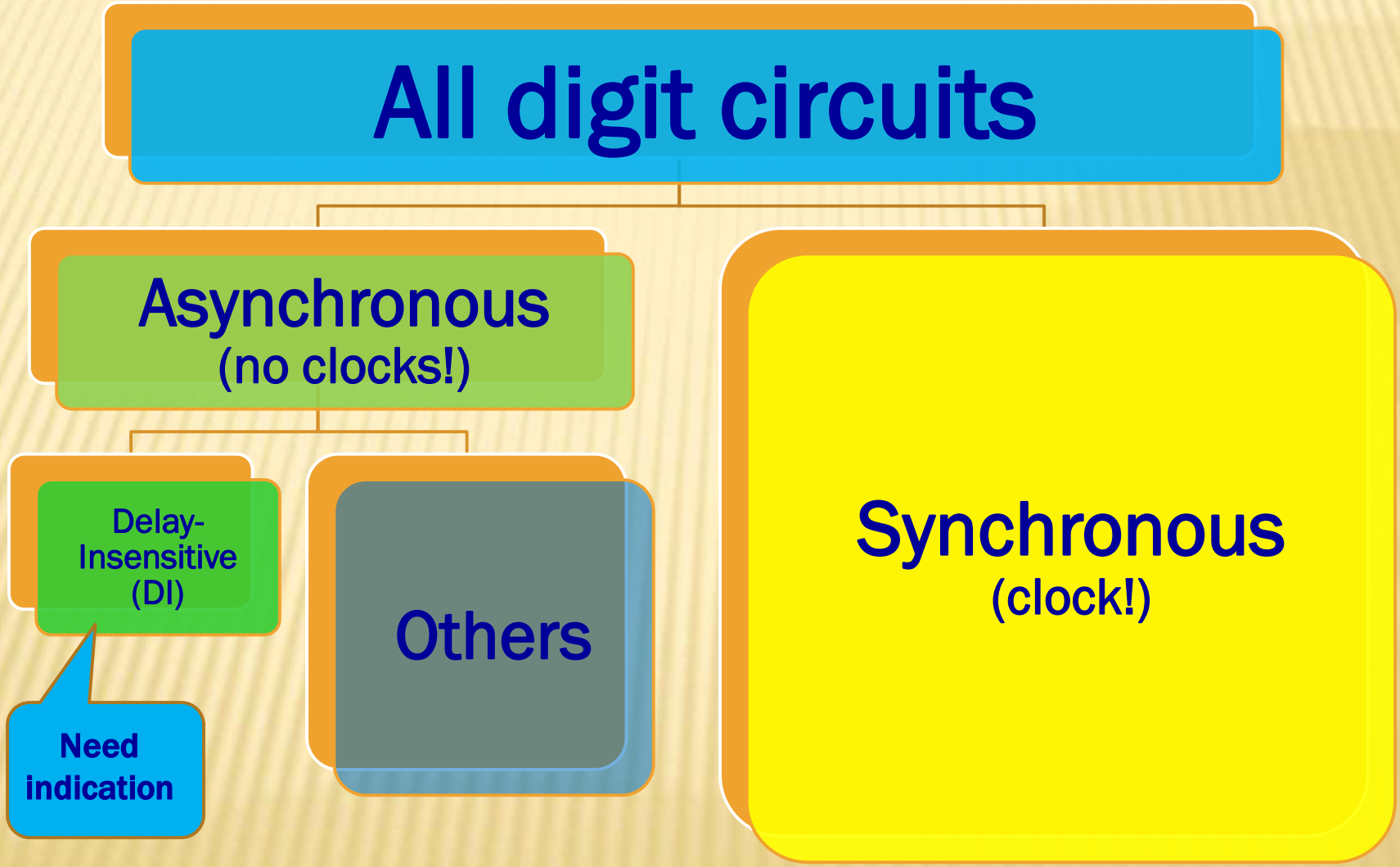
Yury Stepchenkov, Yury Diachenko,
Yury Rogdestvenski, Yury Shikunov,
and Denis Diachenko

Institute of Informatics Problems, Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences, IPI RAS, Moscow, Russian Federation

OUTLINE

- What are the Self-Timed circuits?
- Indication circuitry
- Indication circuit optimization
- Comparison of the indication circuit implementations
- Conclusions

CIRCUITS CLASSIFICATION



ADVANTAGES OF DI CIRCUITS

- Their workability does not depend on delay of their cells and wires
- Free of hazards
- Extremely wide workability range on supply voltage and ambient temperature,
- Constant failure detection terminating any work

DELAY-INSENSITIVE PRINCIPLES

- Two operation phase:
  - work phase (data processing)
  - spacer (pause)
- Self-timed signal coding
- Full indication of all cells in the circuit in each phase of work

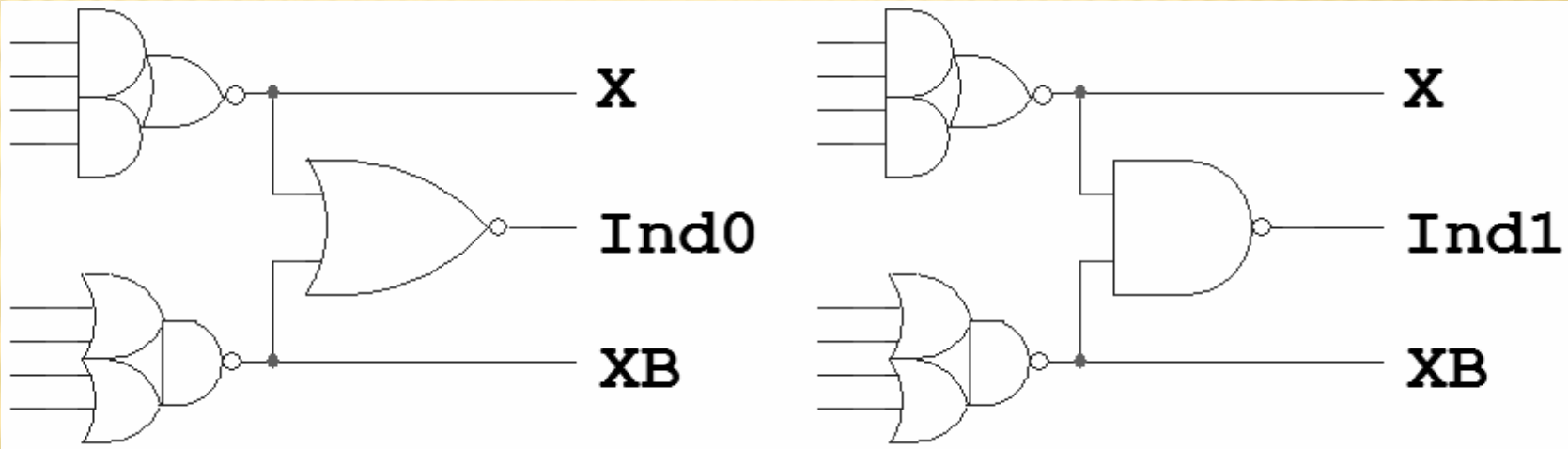
SELF-TIMED CODING

Dual-rail coding: each signal *X* is presented by a pair {*X*, *XB*}

X	XB	Value
0	0	Null spacer
0	1	“0”
1	0	“1”
1	1	Unit spacer

CIRCUIT INDICATION (1)

Combinational circuits:
indicator reflects a dual-rail signal's state

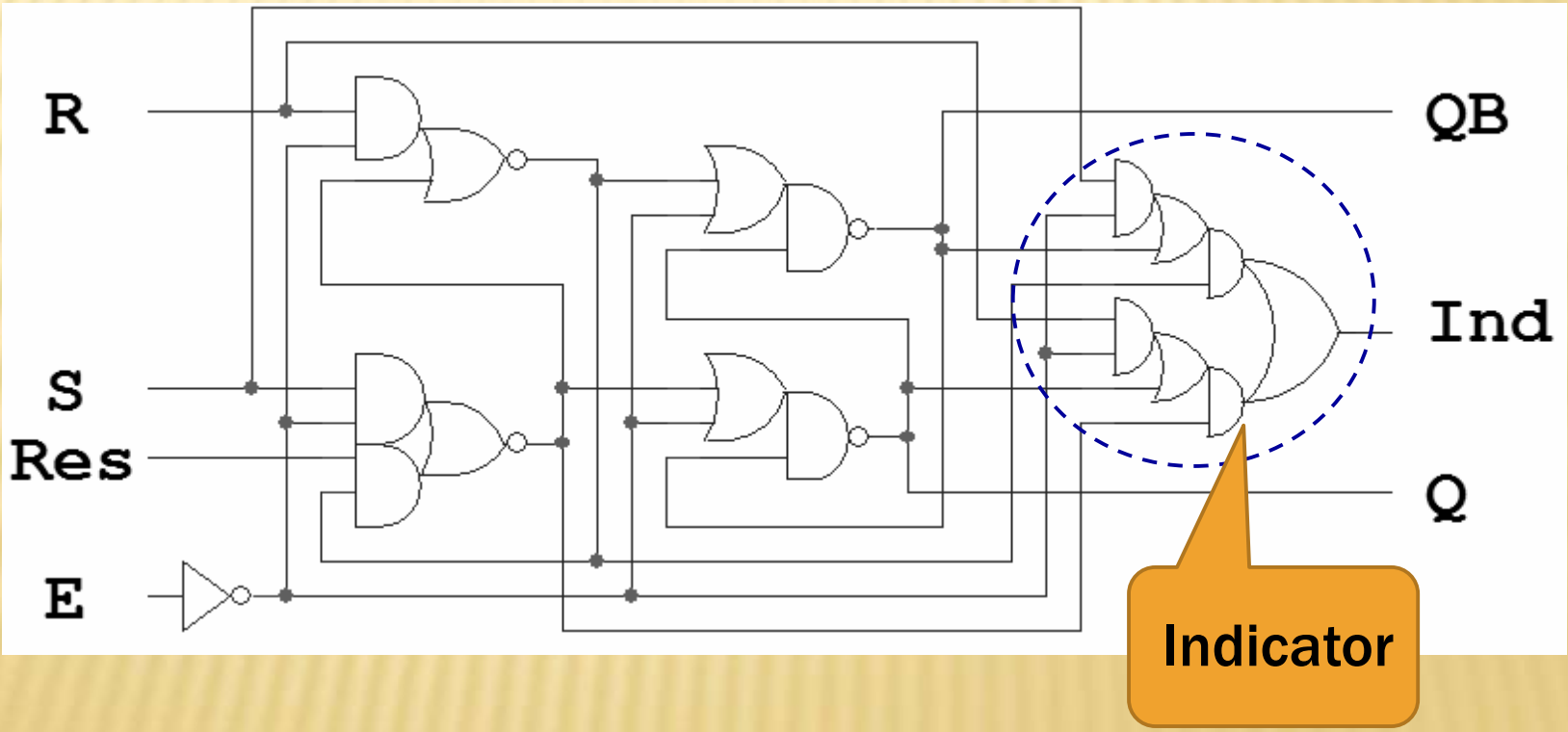


Null spacer **Unit spacer**

CIRCUIT INDICATION (2)

Triggers:

indicator reflects the correspondence between inputs, intermediate signals, and outputs



INDICATION CIRCUITRY (1)

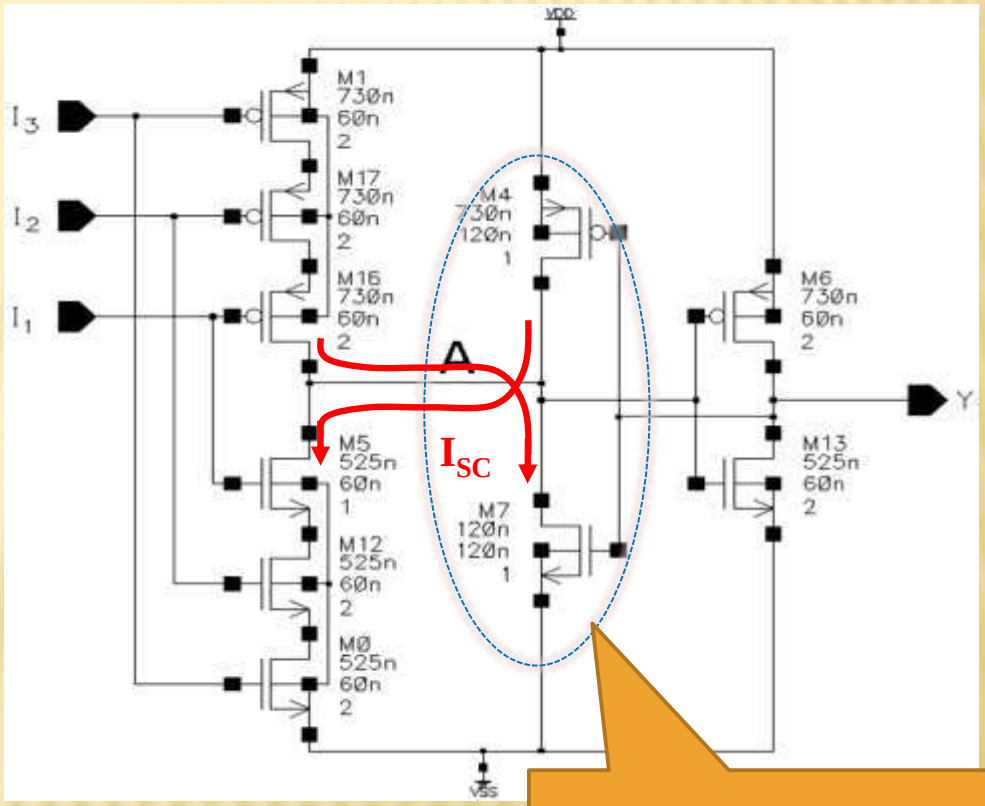
Semi-static Maller's element

Advantages:

- Low complexity:
  2(N+2) transistors,
  $N \leq 3$
- Unit input capacitance

Disadvantages:

- Short-circuit current at each switch
- Low noise immunity



Compression ratio ≤ 3

INDICATION CIRCUITRY (2)

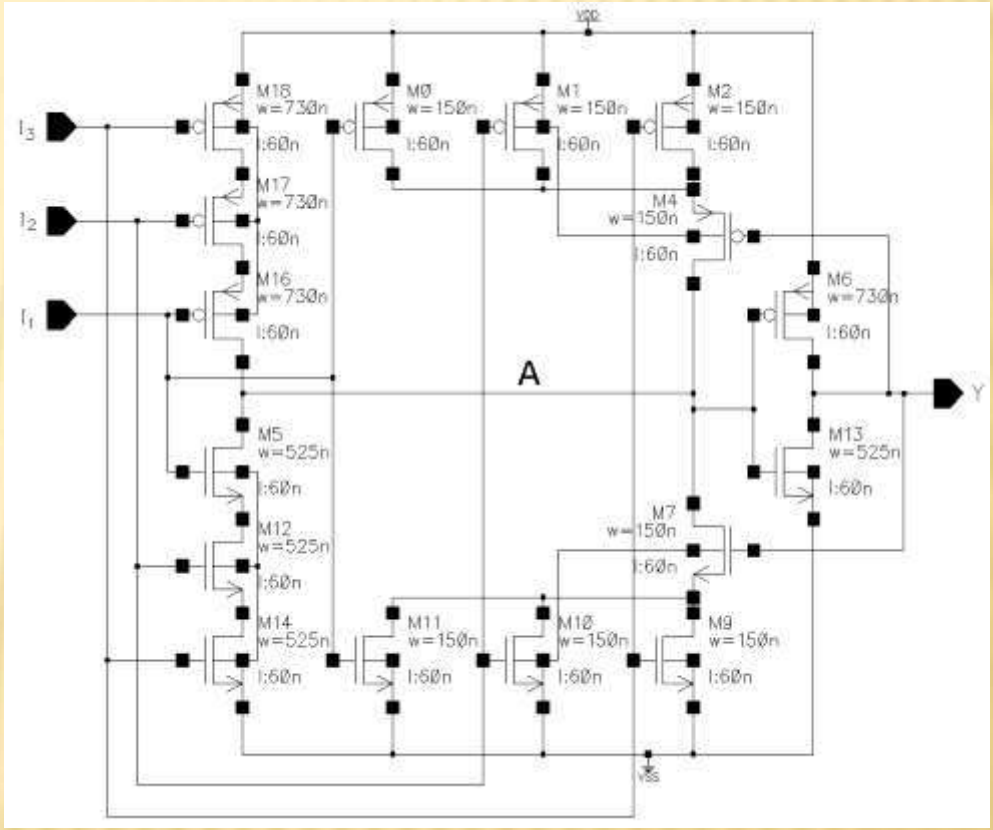
Hysteretic trigger

Advantages:

- No short-circuit current
- High noise immunity

Disdvantages:

- High complexity:
  4(N+1) transistors,
  $N \leq 3$
- Double input capacitance



Compression ratio ≤ 3

INDICATION CIRCUITRY (3)

Multi-input Hysteretic trigger

Advantages:

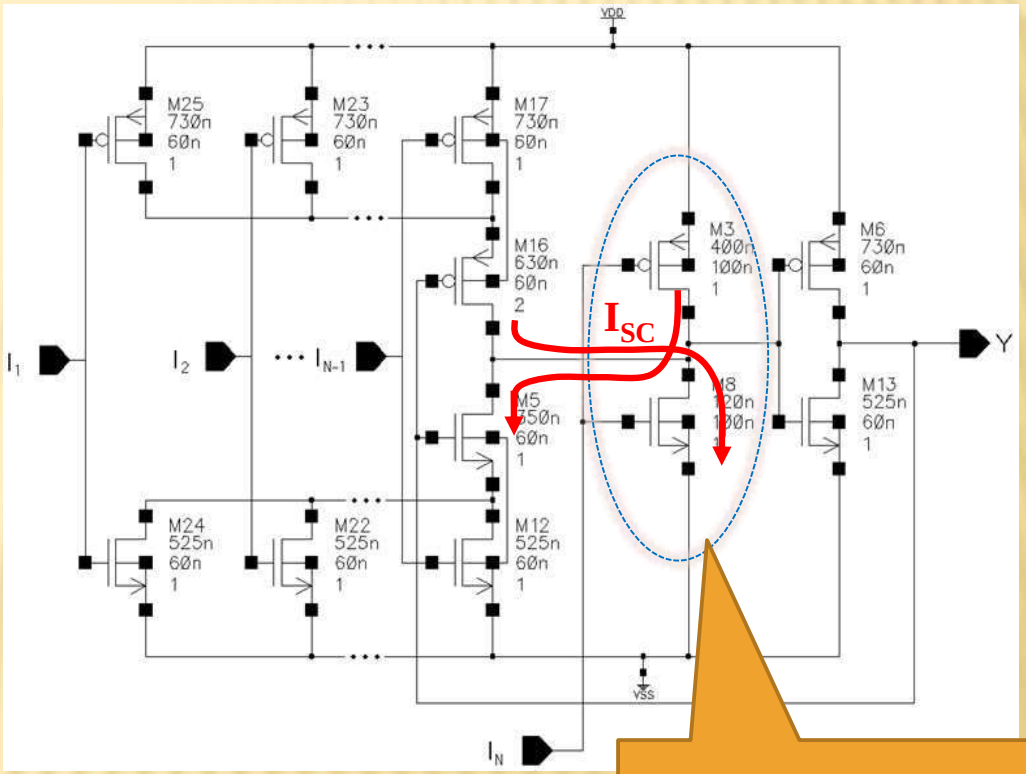
- Low complexity:
  2(N+2) transistors,
  any N
- Unit input capacitance
- High compression ratio

Disadvantages:

- Short-circuit current

only in worst case

- Low noise immunity



Compression ratio > 9

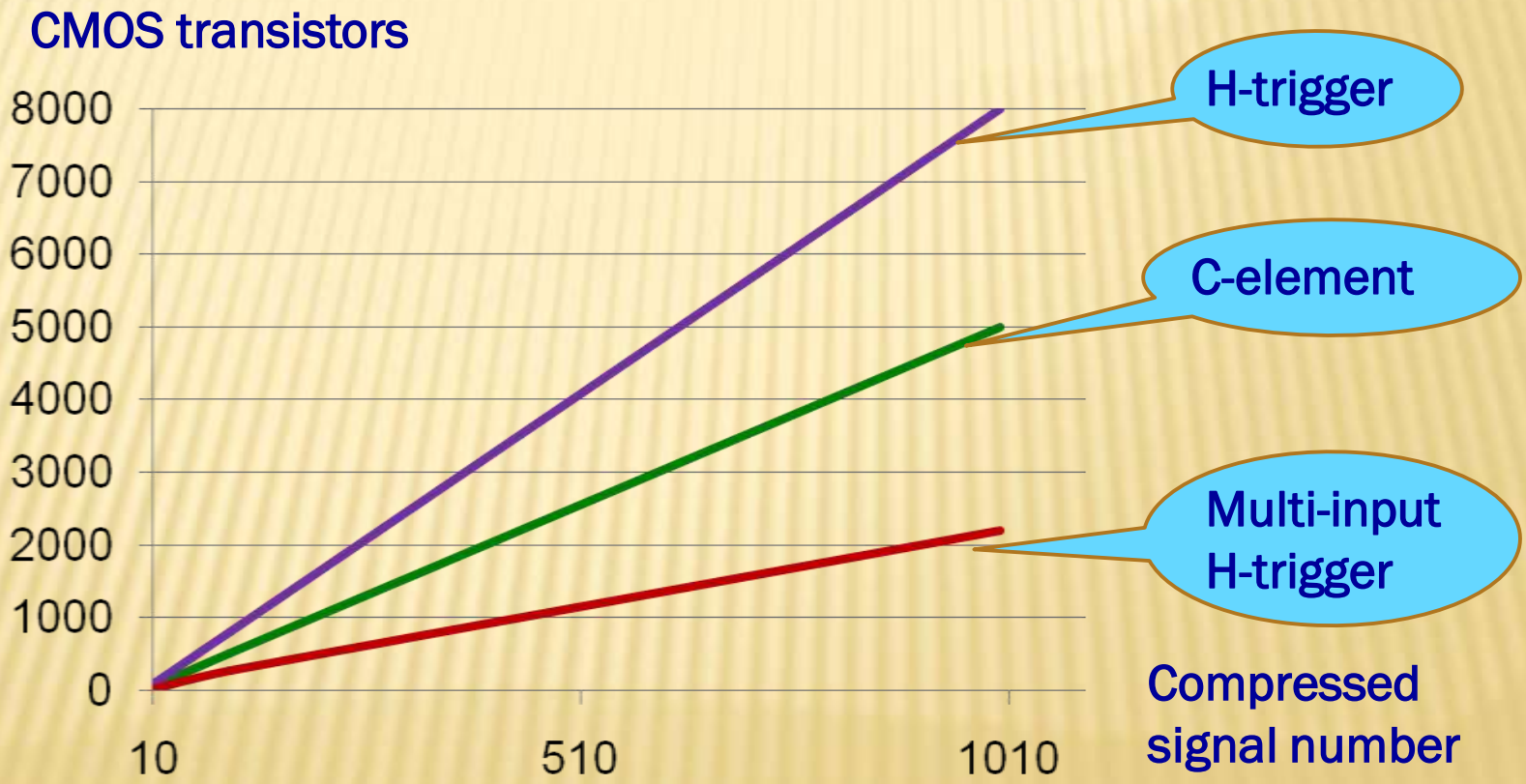
INDICATION COMPLEXITY (1)

Complexity of an indication circuit implemented on various bases in CMOS transistors

Implementation base	Number of compressed indication signals		
	10	100	1000
C-element	48	504	4998
H-trigger	76	804	7996
Multi-input H-trigger	24	264	2196

INDICATION COMPLEXITY (2)

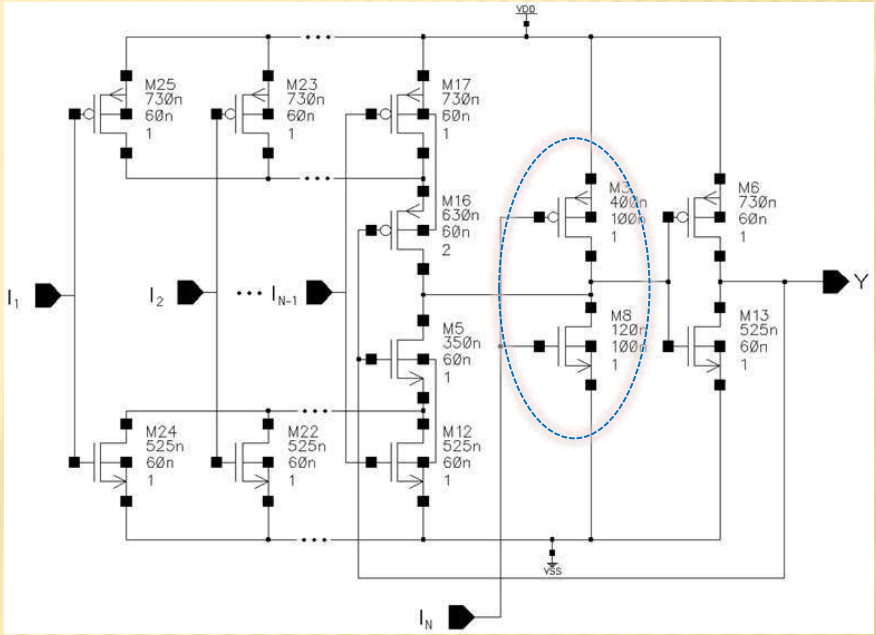
Complexity in CMOS transistors vs compressed signal number on various bases



MULTI-INPUT H-TRIGGER (1)

Workability conditions

$$\begin{cases} \dfrac{L_{p,weak}}{W_{p,weak}} \geq K_{p,HM} \cdot \left(\dfrac{L_{n,in}}{W_{n,in}} + \dfrac{L_{n,FB}}{W_{n,FB}} \right) \\ \dfrac{L_{n,weak}}{W_{n,weak}} \geq K_{n,HM} \cdot \left(\dfrac{L_{p,in}}{W_{p,in}} + \dfrac{L_{p,FB}}{W_{p,FB}} \right) \end{cases}$$

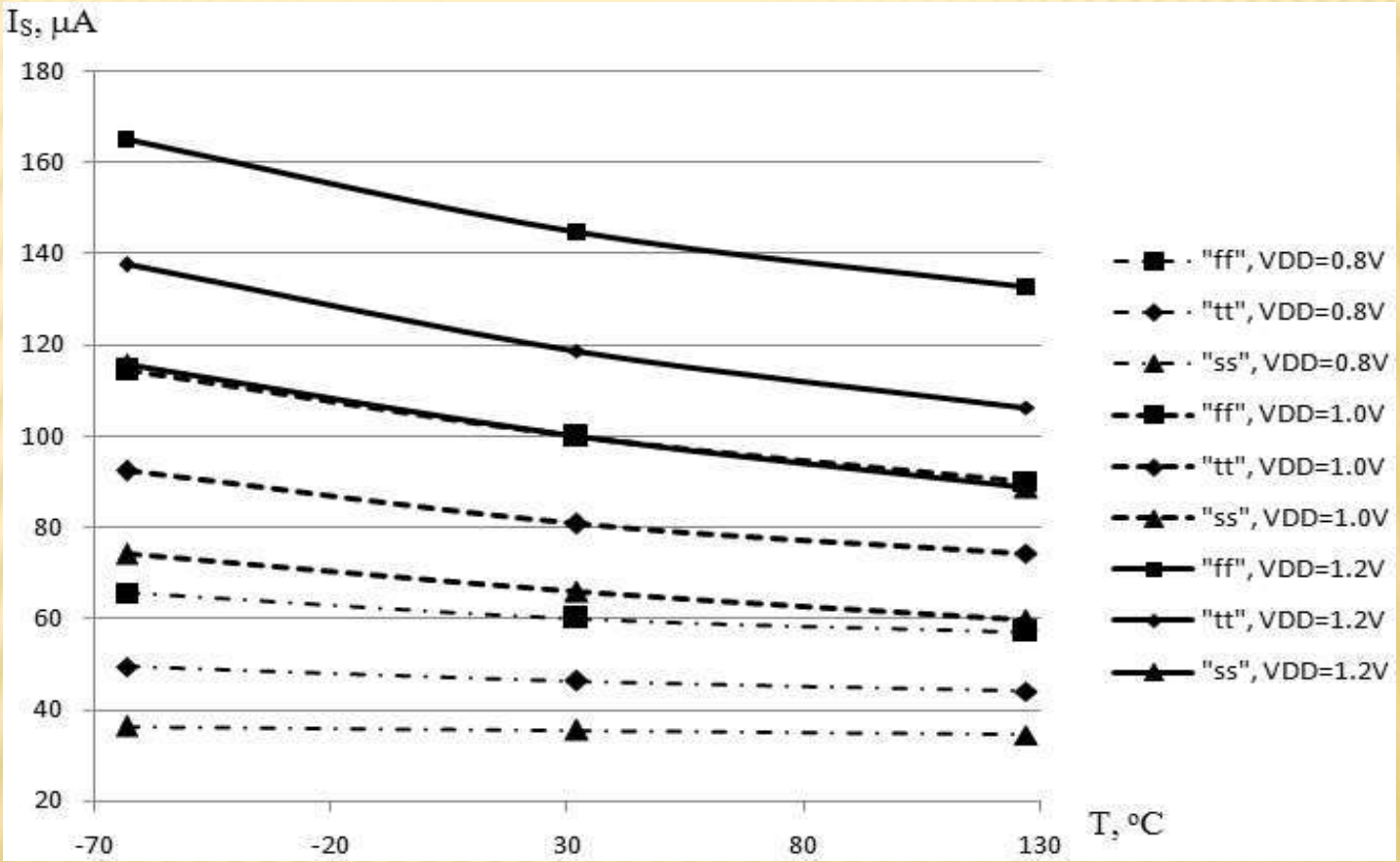


For standard 65-nm CMOS process

$$K_{n,HM} = 6.4; K_{p,HM} = 0.9$$

MULTI-INPUT H-TRIGGER (2)

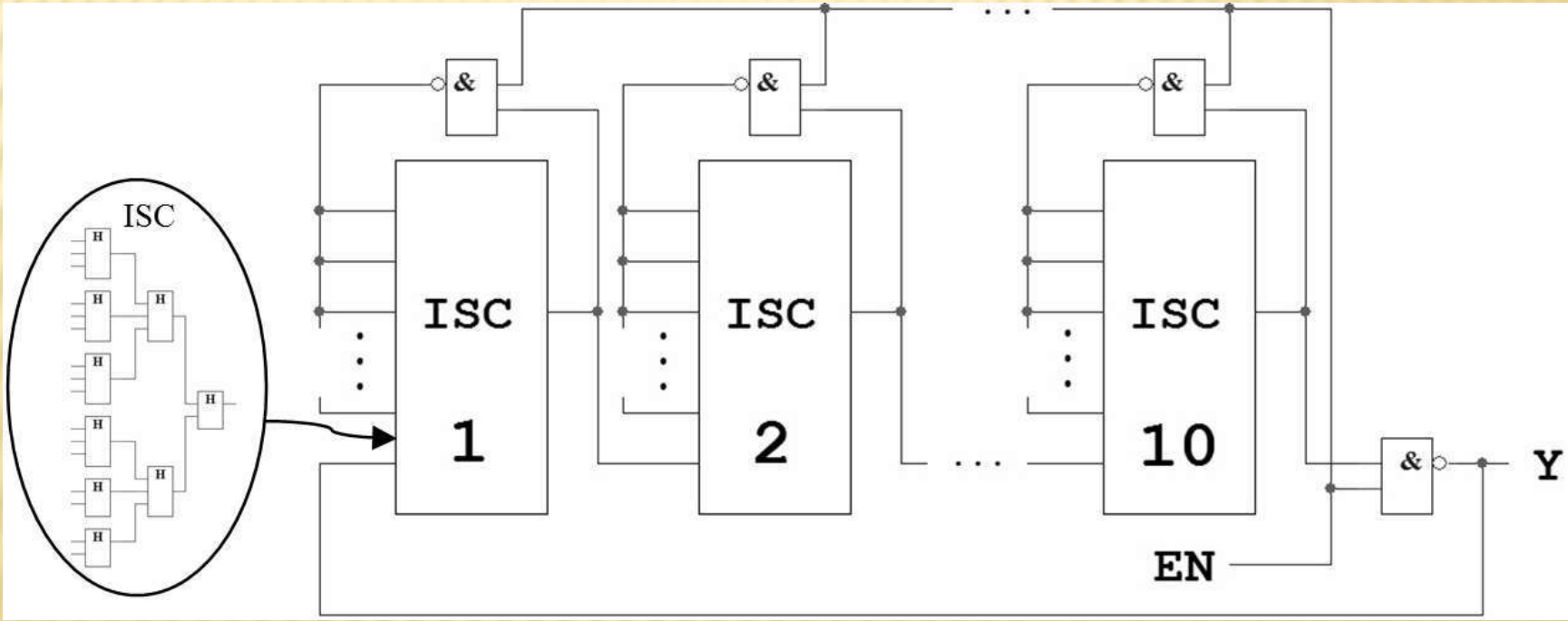
Short-circuit current in worst case for 16-input H-trigger



INDICATION CIRCUIT DELAYS (1)

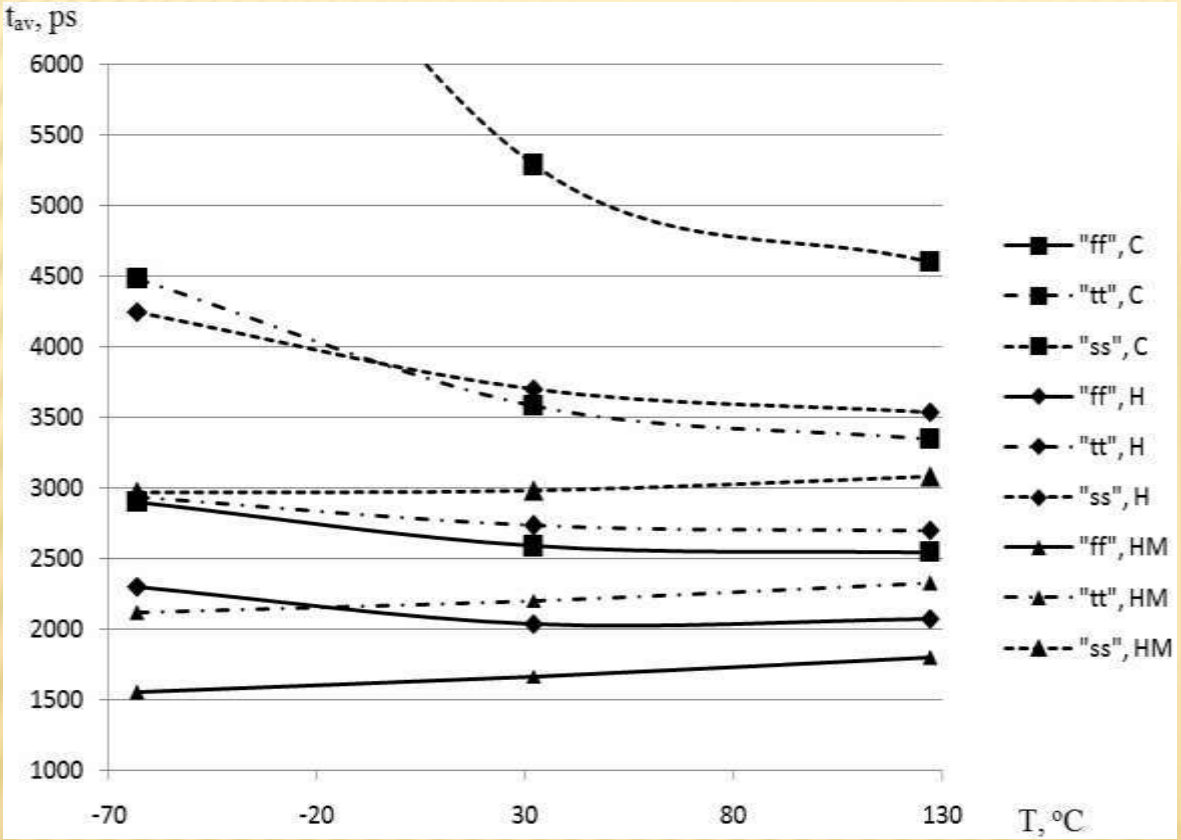
Simulation basis:

- Spectre (Cadence)
- Ring oscillator



INDICATION CIRCUIT DELAYS (2)

Oscillation periods for M = 16, V_{DD} = 0.8V



***Legend*:**

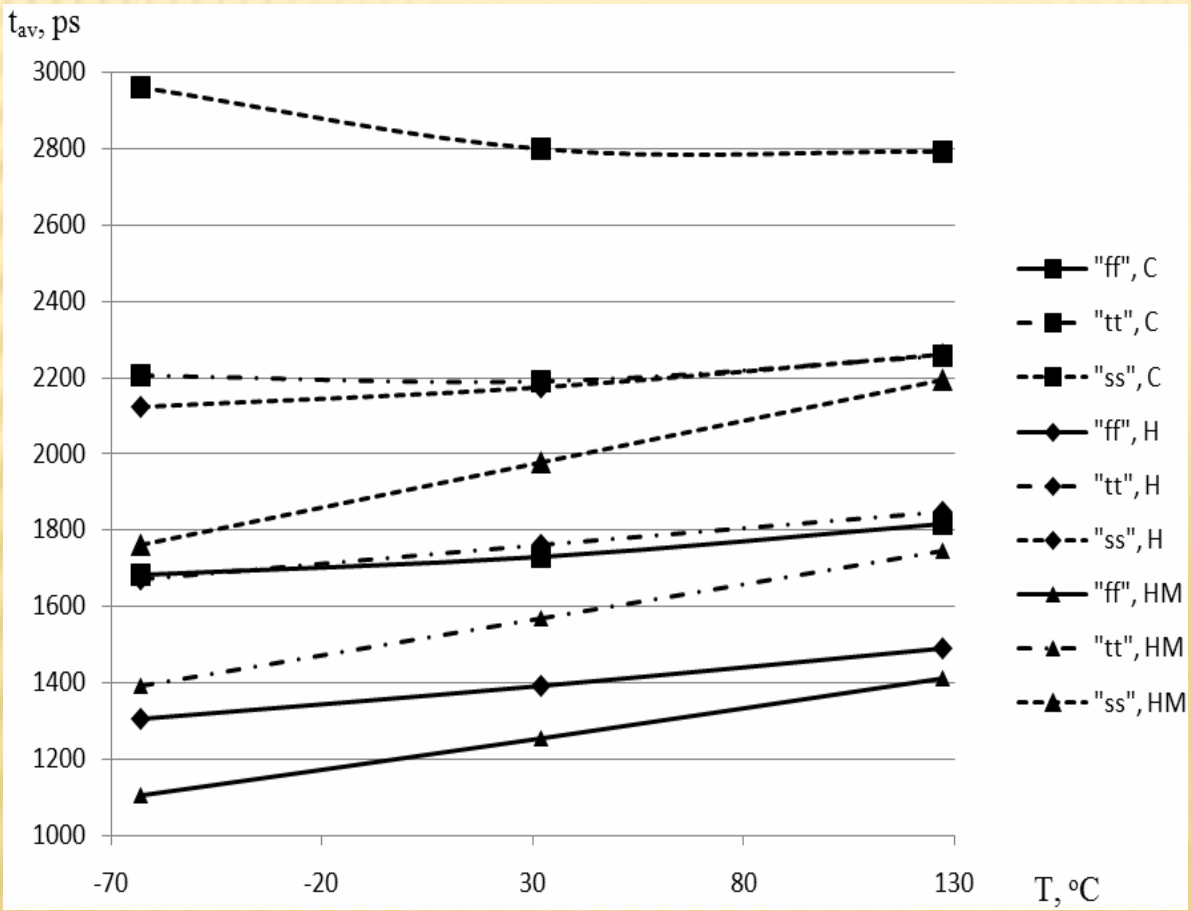
"C" = C-element

"H" = H-trigger

"HM" = Multi-input H-trigger

INDICATION CIRCUIT DELAYS (3)

Oscillation periods for M = 16, V_{DD} = 1.0V



***Legend*:**

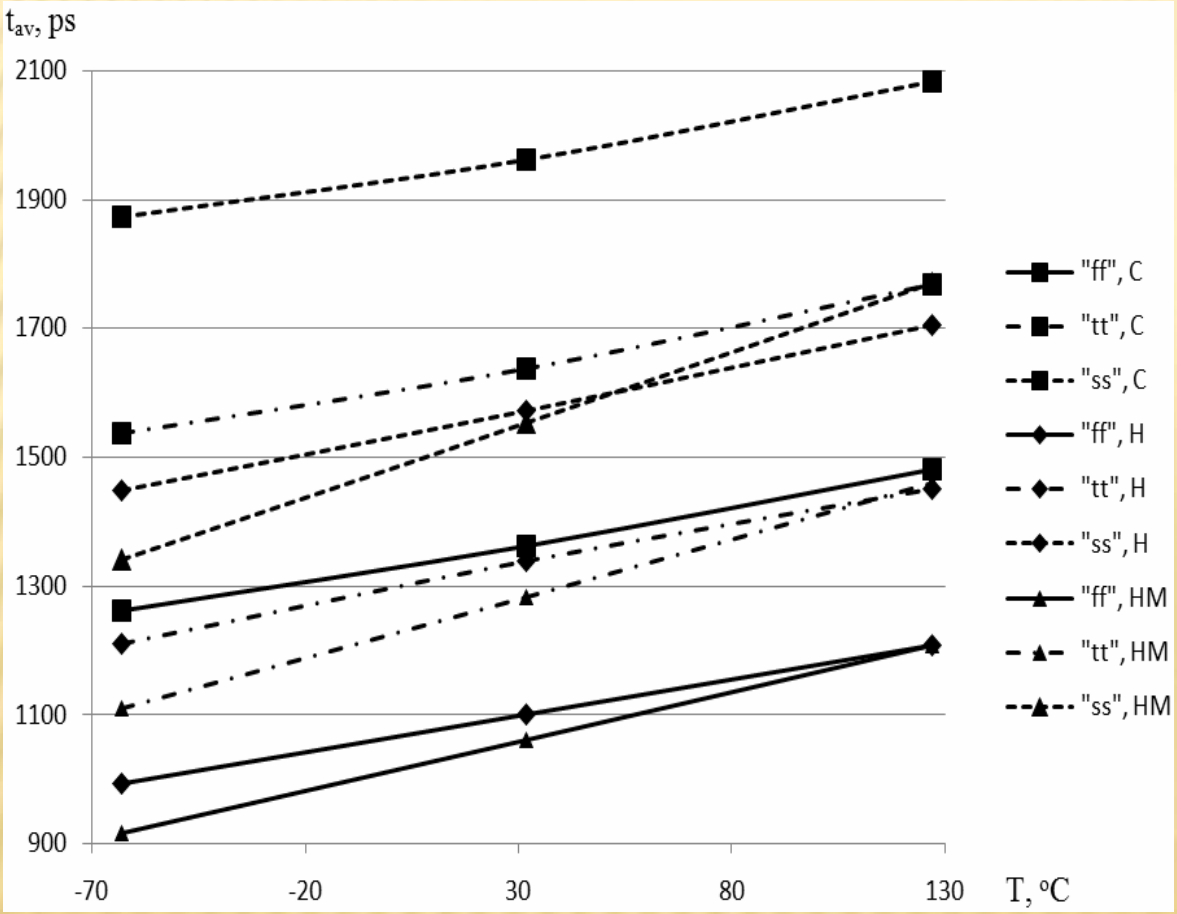
"C" = C-element

"H" = H-trigger

"HM" = Multi-input H-trigger

INDICATION CIRCUIT DELAYS (4)

Oscillation periods for M = 16, V_{DD} = 1.2V



***Legend*:**

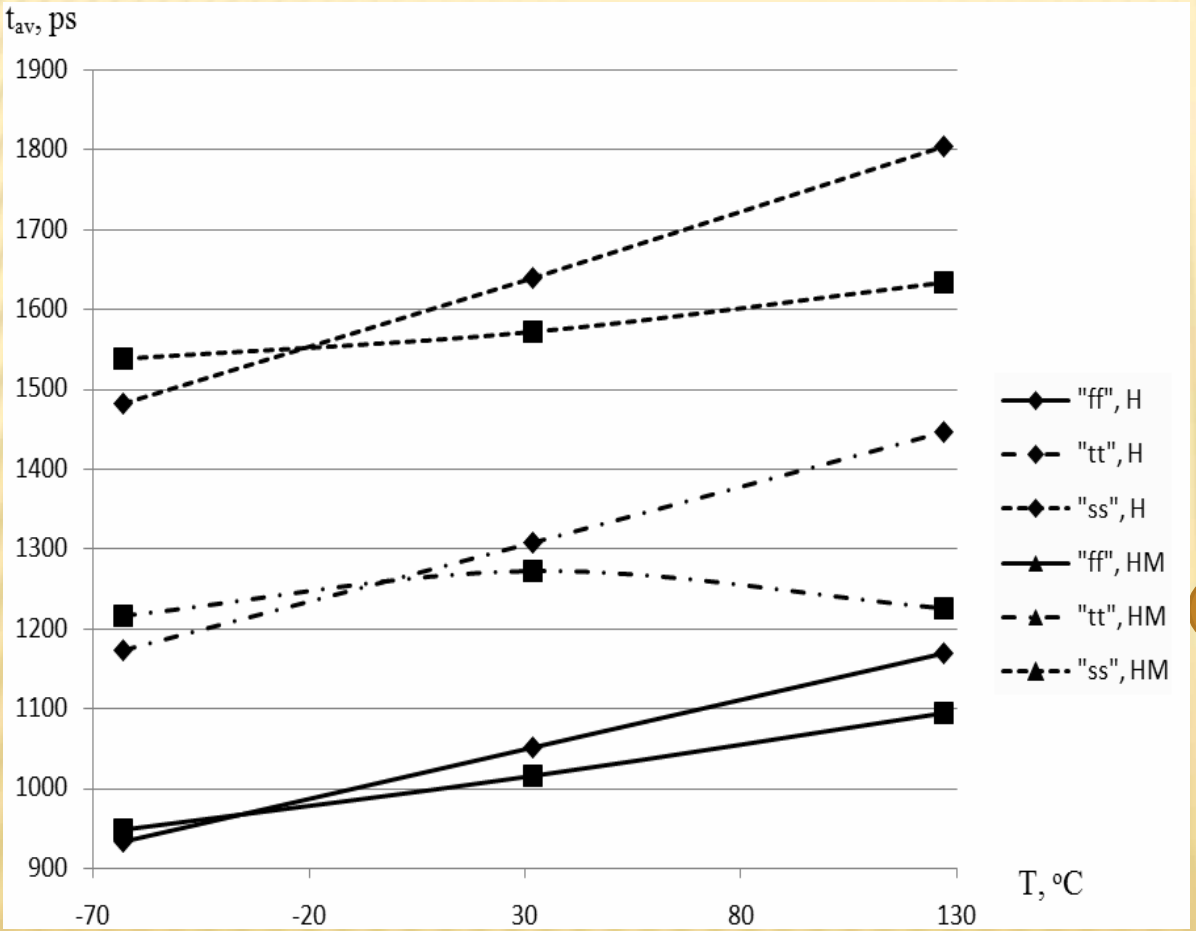
"C" = C-element

"H" = H-trigger

"HM" = Multi-input H-trigger

INDICATION CIRCUIT DELAYS (5)

Oscillation periods for M = 9, V_{DD} = 1.0V



***Legend*:**

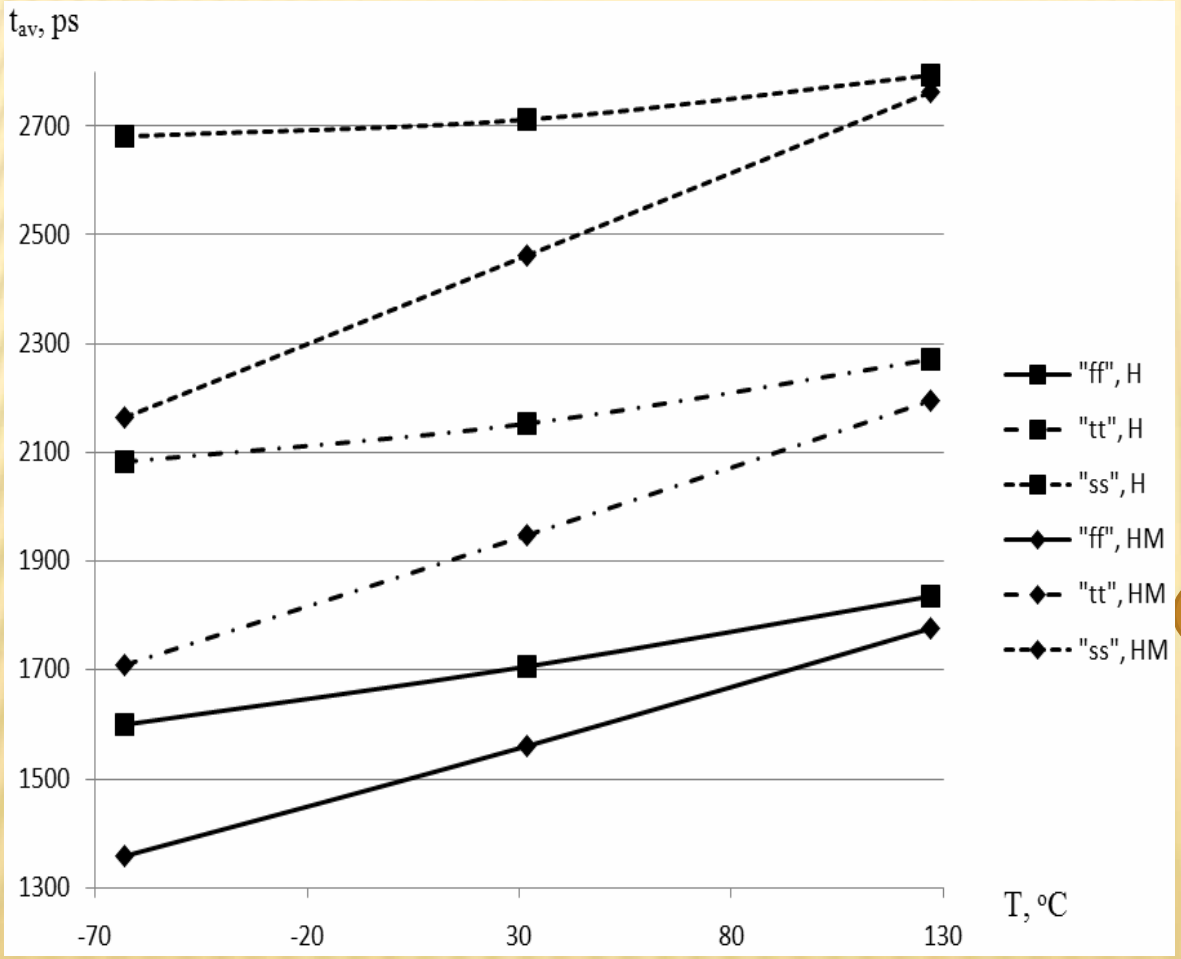
"C" = C-element

"H" = H-trigger

"HM" = Multi-input H-trigger

INDICATION CIRCUIT DELAYS (6)

Oscillation periods for M = 27, V_{DD} = 1.0V



***Legend*:**

"C" = C-element

"H" = H-trigger

"HM" = Multi-input H-trigger

SUMMARY

- Multi-input H-triggers allow both for reducing hardware costs of the indication subcircuit implementation by several times, and for decreasing its delay by one and a half times compared to conventional H-triggers.
- C-element demonstrates the worst performance in comparison with both conventional H-trigger and multi-input H-trigger.
- Varying the size of transistors in the multi-input H-trigger circuit allows for shifting balance between its short-circuit current and performance in any direction. One can accelerate H-trigger at the expense of increasing allowable short-circuit current or reduce possible short-circuit current, due to deterioration in its performance.

Thank You!

CONTACTS

- Director: academician Sokolov I.A.
- Address: Institute of Informatics Problems of the Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences (IPI RAS), Moscow, Russian Federation, 119333,
  Vavilova str., 44, b.2
- Tel: +7 (495) 137 34 94
- Fax: +7 (495) 930 45 05
- E-mail: lSokolov@ipiran.ru
- Stepchenkov Y.A., tel. +7 (495) 671 15 20, Ystepchenkov@ipiran.ru