SPEED-INDEPENDENT FUSED MULTIPLY ADD AND SUBTRACT UNIT

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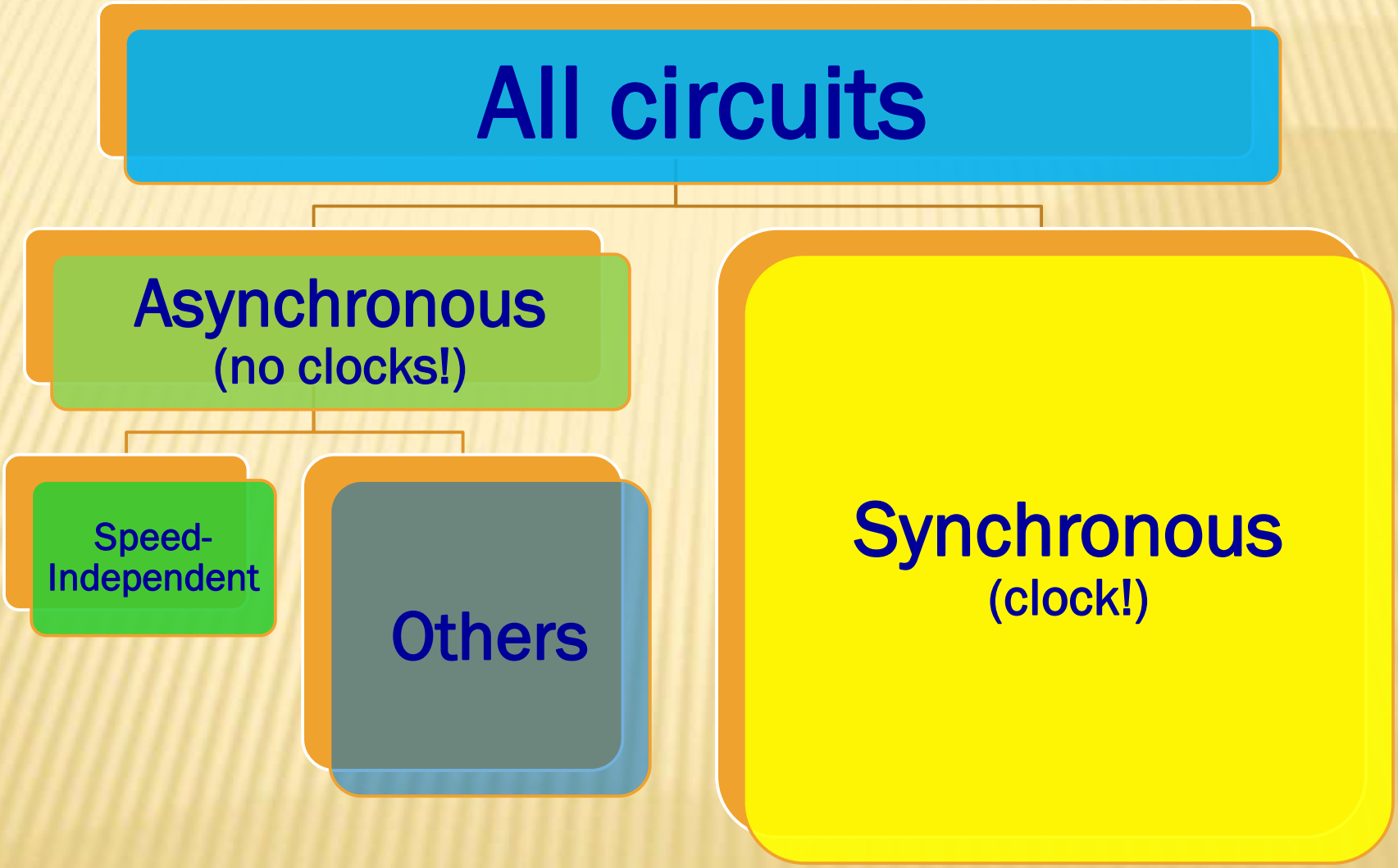
OUTLINE

- **What circuits do we design?**
- **Block diagram of Fused Multiply-Add & Subtract** (SI-FMAS) Unit
- **Simplified indication**
- **SI-FMAS implementation**
- **Testing SI-FMAS**
- **Conclusions**

CIRCUITS CLASSIFICATION



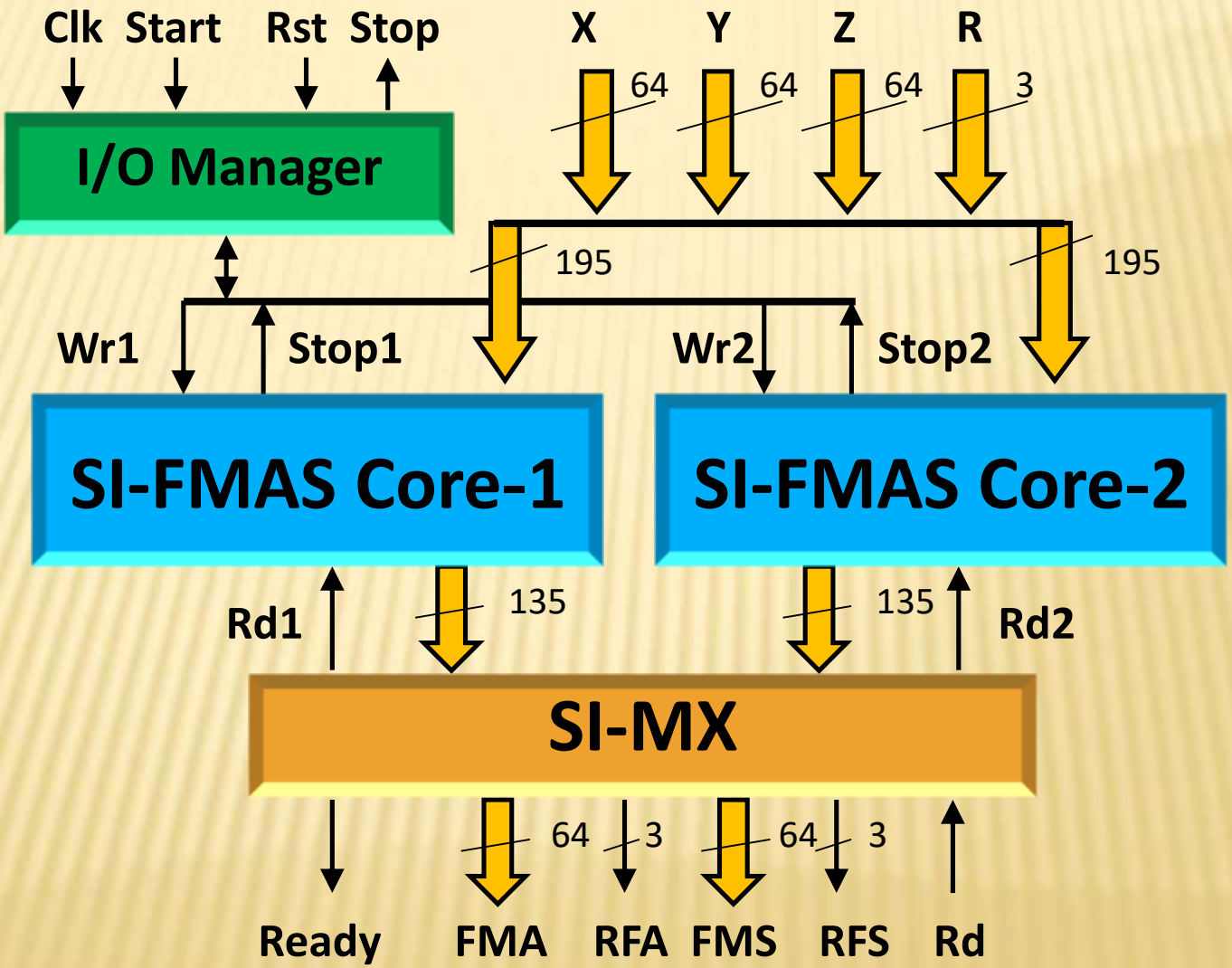
ADVANTAGES OF SI CIRCUITS

- Their workability does not depend on delay of their cells
- They are free of hazards
- They have extremely wide workability range on supply voltage and ambient temperature,
- They detect constant failures and stop working

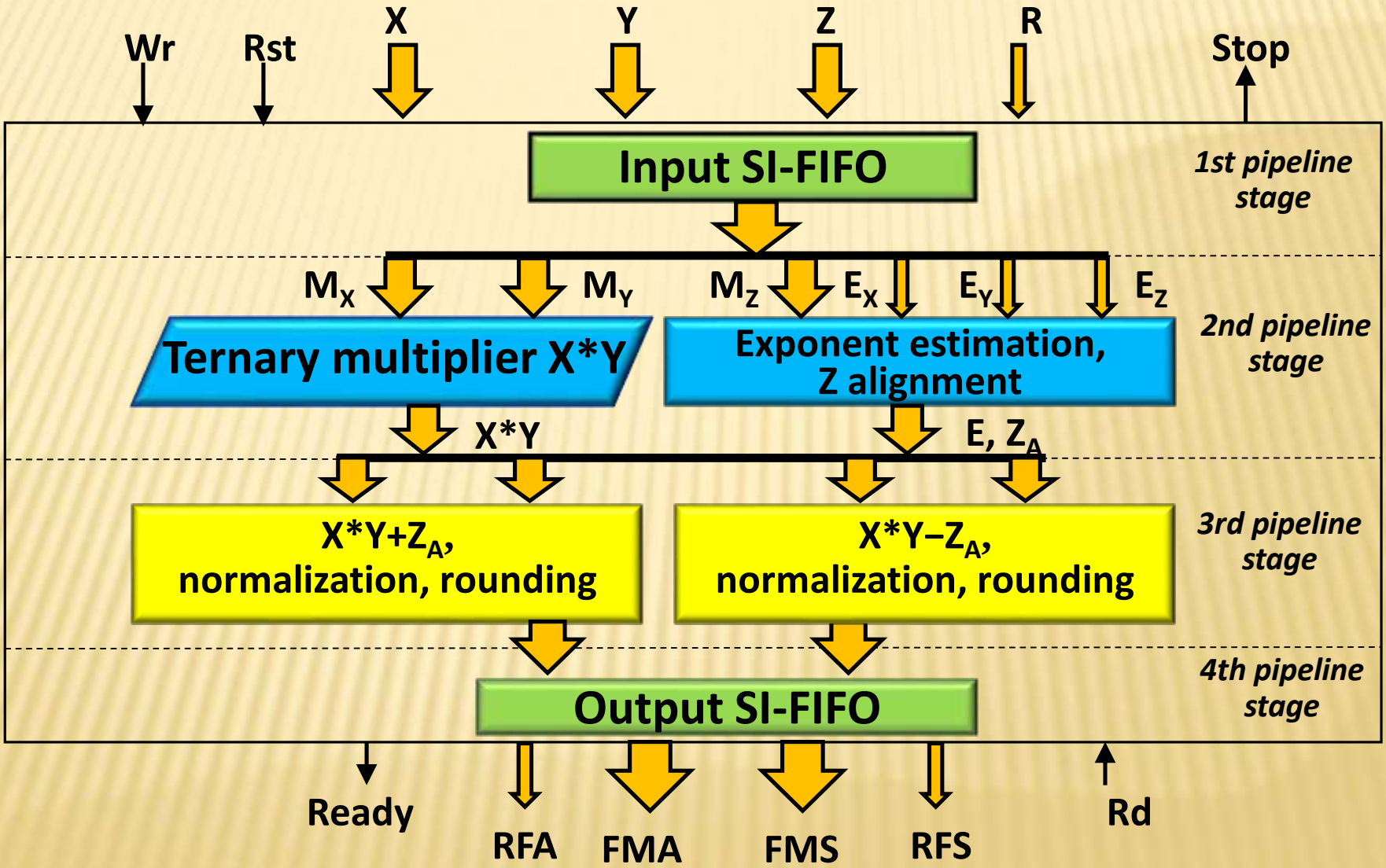
SPEED-INDEPENDENT PRINCIPLES

- Two phase operation: work and spacer (pause)
- Each circuit cell can switch only once during transient of the circuit from spacer to next work state
- Full indication of all cells in the circuit in each phase of work

BLOCK DIAGRAM OF SI-FMAS



BLOCK DIAGRAM OF SI-FMAS CORE



SIMPLIFIED INDICATION (1)

Why is it possible?

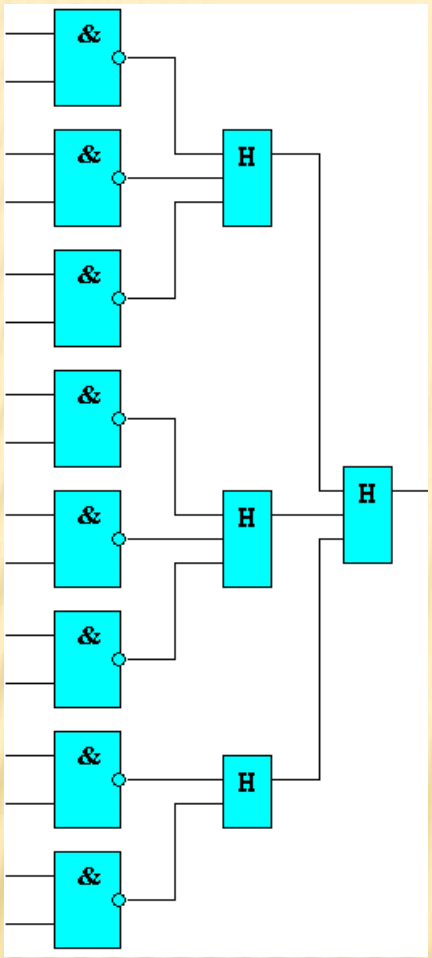
- First work state just appeared at circuit's outputs during transient from spacer to work phase is a stationary state
- CMOS cell stops its switching into opposite state if input combination that caused this transient has disappeared

SIMPLIFIED INDICATION (2)

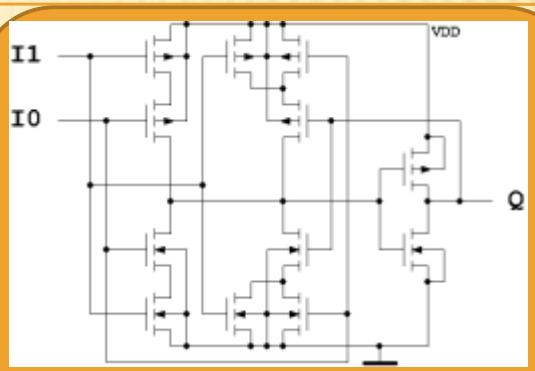
How can we optimize indication?

- **Full indication in spacer phase and simplified one in work phase**
- **Bitwise indication in combinational circuits**
- **Taking into account bitwise indicators in the input register of the following pipeline stage**

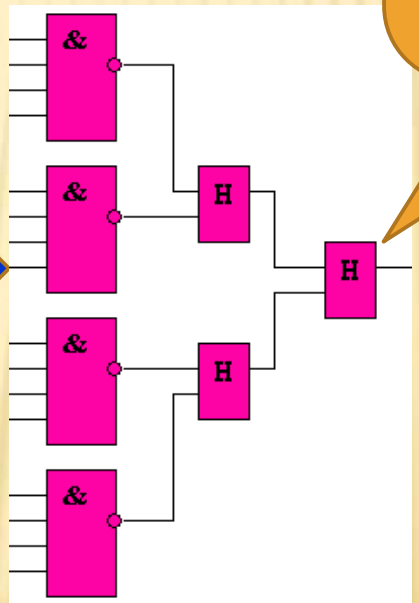
SIMPLIFIED INDICATION (3)

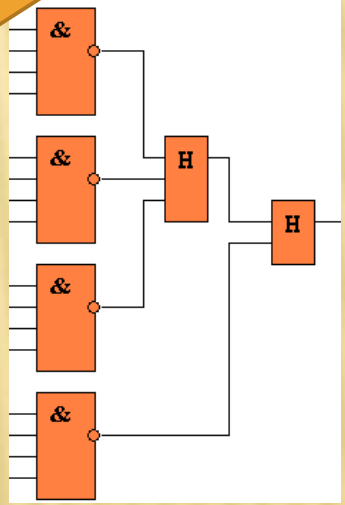


Unit spacer



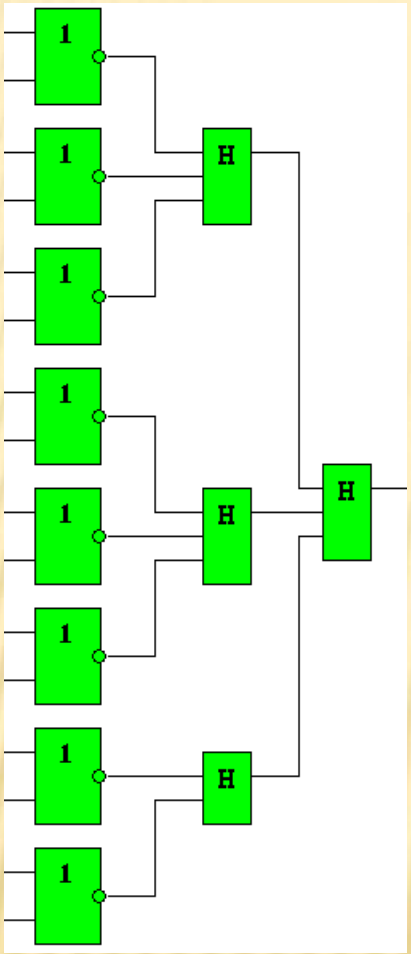
$Q^+ = I0*I1 + Q*(I0 + I1)$



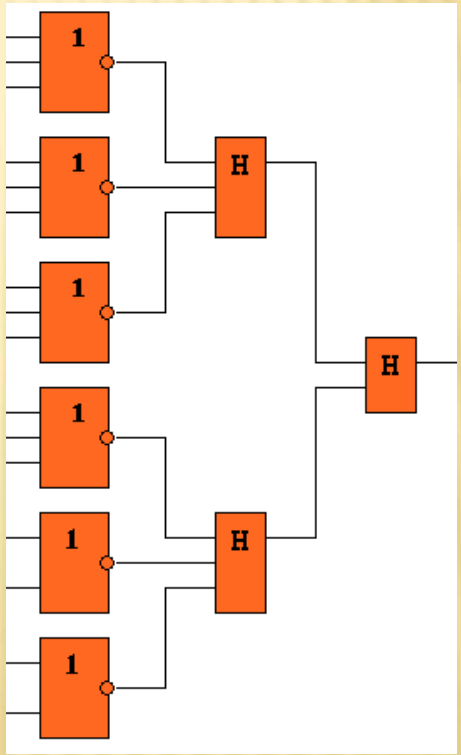


CMOS transistors: **92** → **68** → **60**

SIMPLIFIED INDICATION (4)

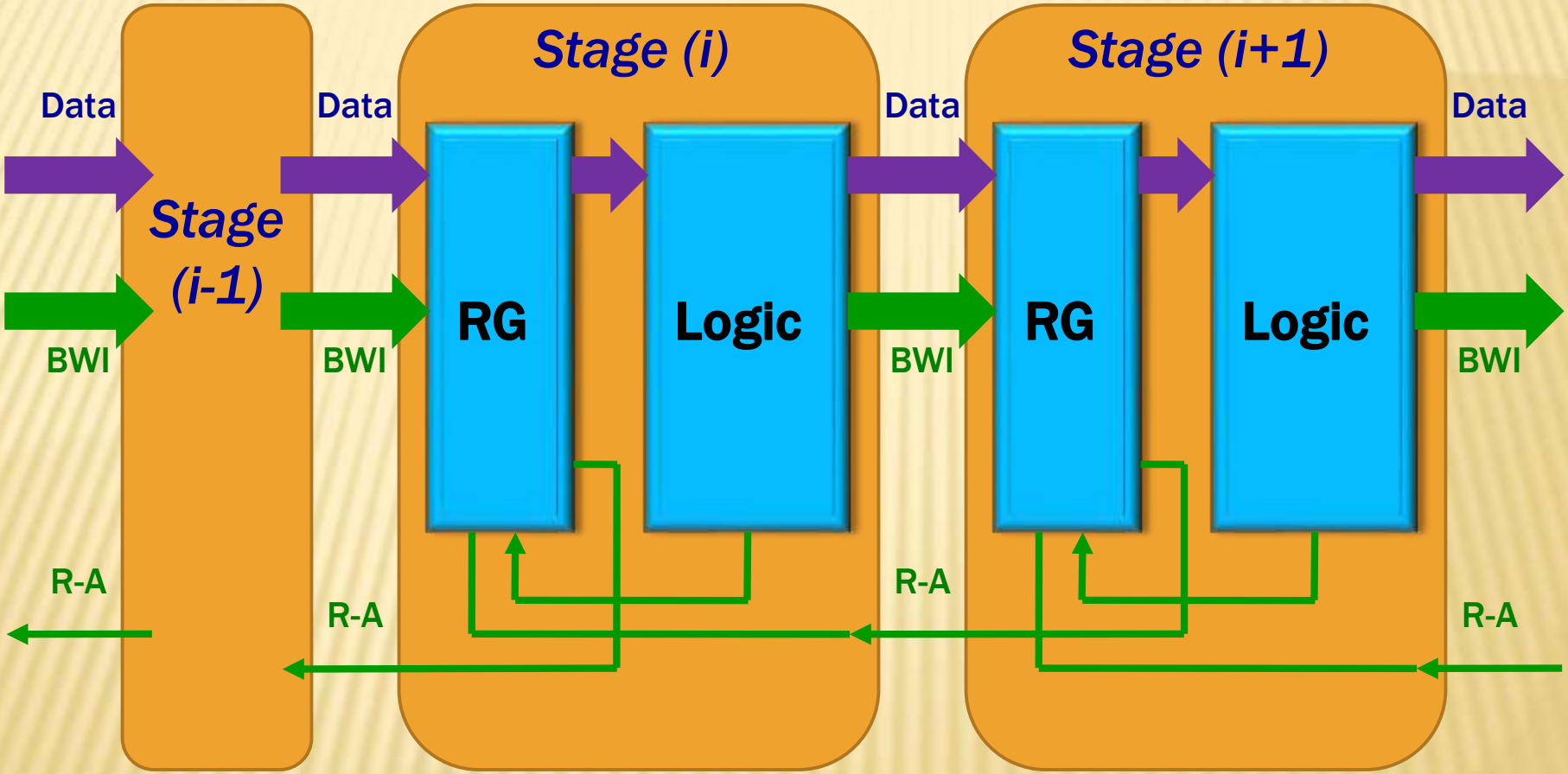


Zero spacer



CMOS transistors: **92** → **76**

OPTIMIZED PIPELINE INDICATION



IMPLEMENTATION BASIS

- **Traditional CMOS circuitry with dual-rail signals everywhere except multiplier utilized ternary coding,**
- 65-nm CMOS process with 6 metals,
- **Standard cell library (Dolphin)**
- **Self-timed cell library (IPI65D, 108 cells) designed in IPI FRC CSC RAS**

FEATURES OF SI-FMAS

Parameter	Synchronous analog	SI-FMAS
Die size, mm^2	0.312	1.12
Performance, Gflops	2.06	3.15
Latency, ns	10.8	1.84
Die size efficiency, mm^2/Gflops	0.151	0.321
Workability range on V_{DD}	$V_{DD} \pm 10\%$	$V_{th}...V_{BD}$

LAYOUT OF SI-FMAS

Input FIFO

Fraction Multiplier

Exponent calculator

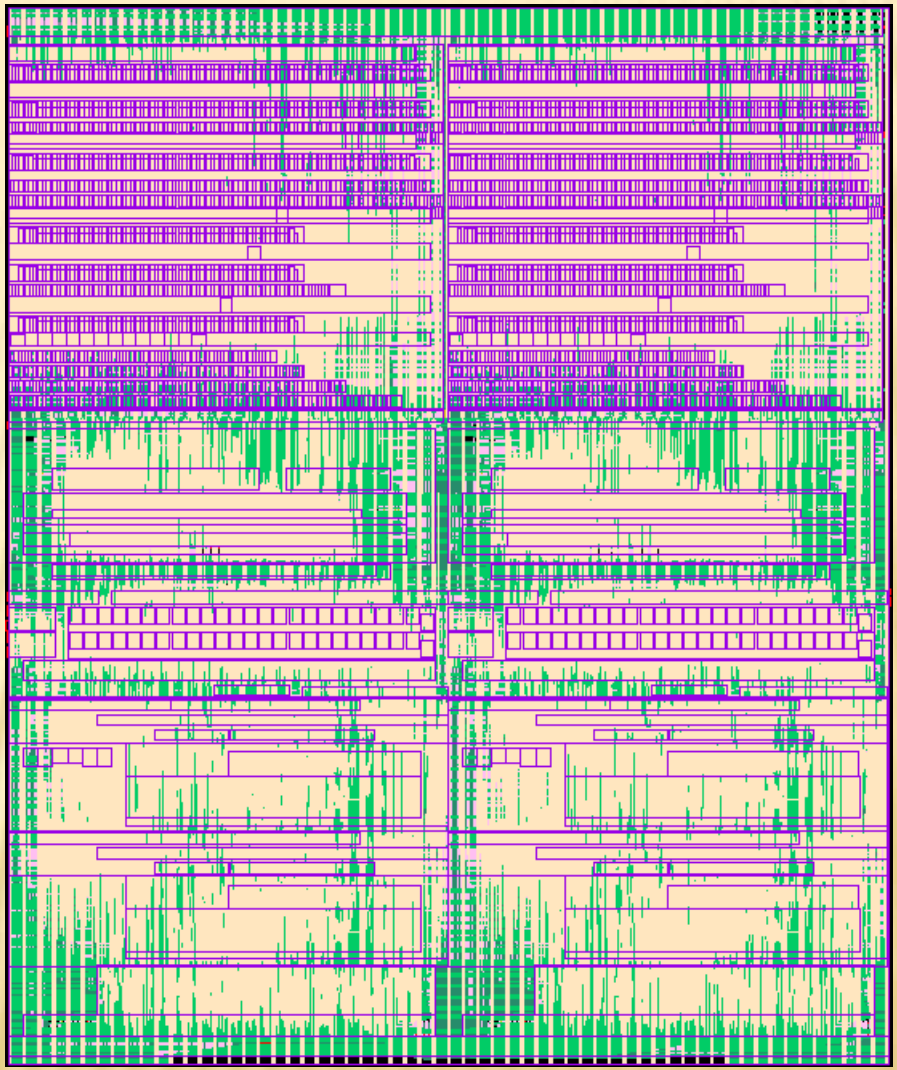
Adder-Subtractor

Normalizer

Round & Post-normalization

Output FIFO

Multiplexer



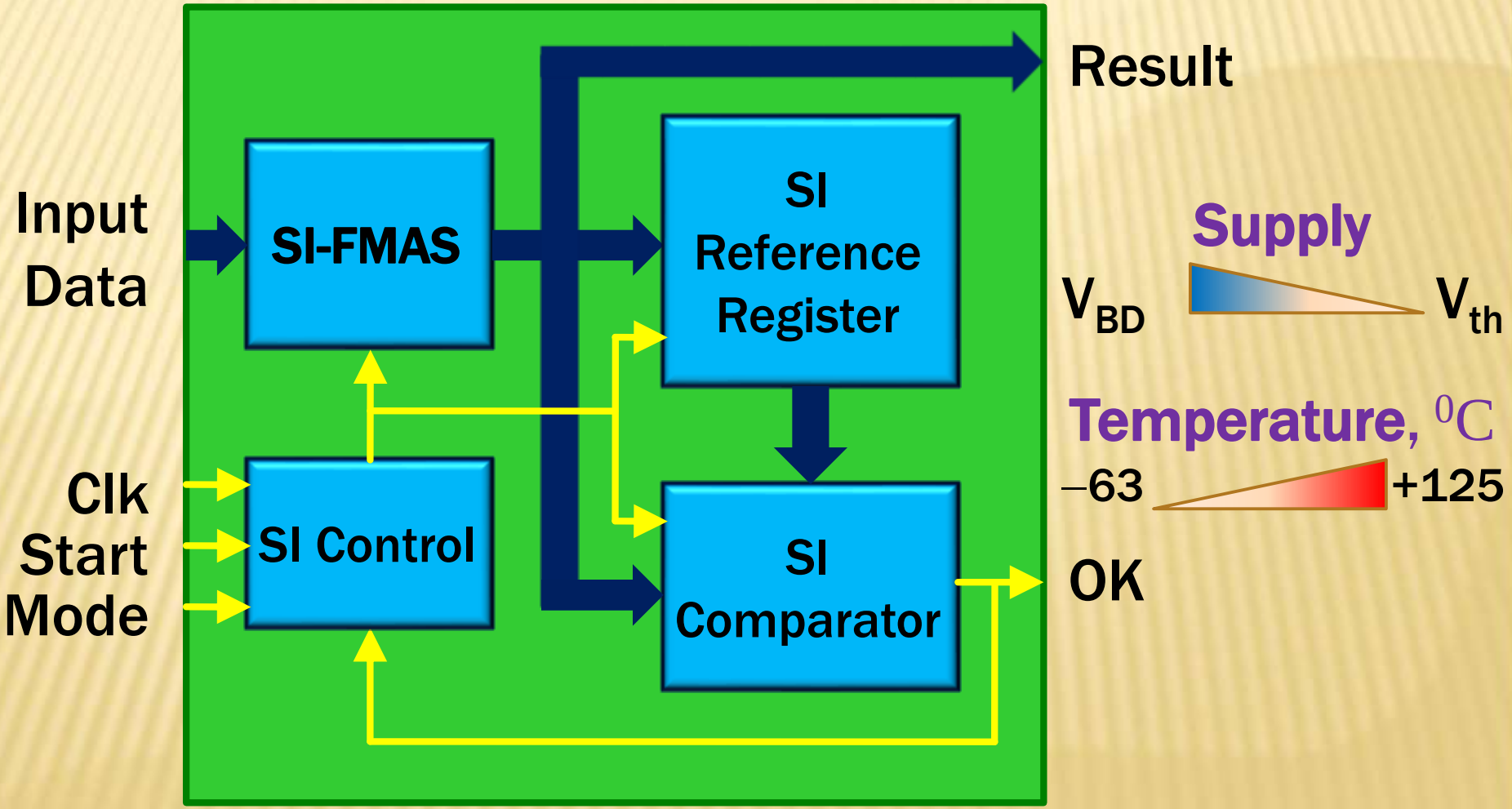
GOALS OF TESTING: *SYNCHRONOUS*

- **Logical Level:**
  - **Functional verification**
- **Electrical Level:**
  - **Eliminating hazards and signal competitions in a full range of supply voltage and temperature**

GOALS OF TESTING: *SPEED-INDEPENDENT*

- **Logical Level:**
  - **Functional** verification
  - **Self-timed analysis (ASPECT, FAZAN, FIESTA)**
- **Electrical Level:**
  -  **Nothing**

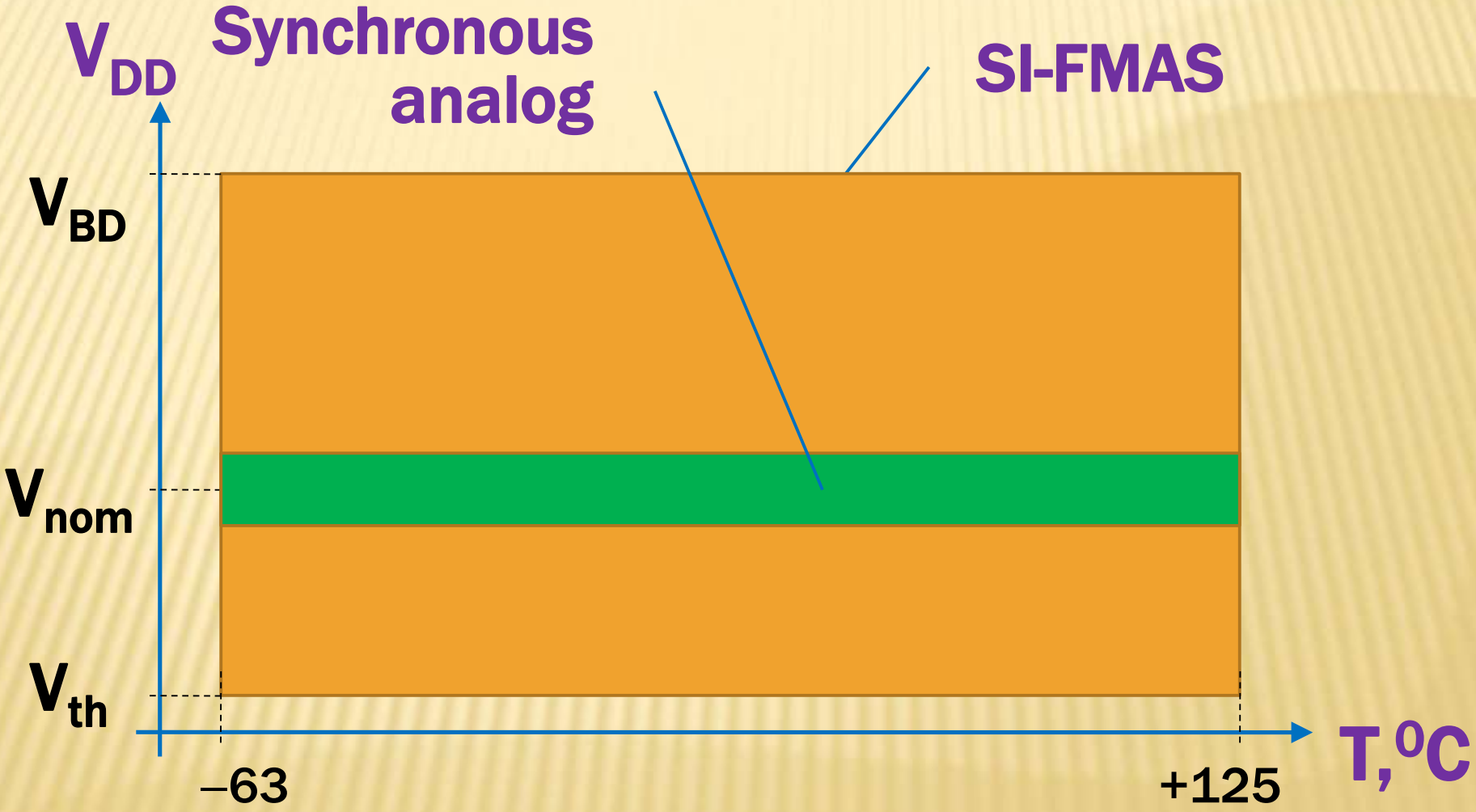
HARDWARE TEST ENVIRONMENT



TEST ORDER

- Supply nominal voltage
- **Set fixed operands at SI-FMAS inputs and Mode=0**
- **Run clock generator and set** Start =1
- **Change input Mode to Mode=1**
- **Observe periodic pulses at output OK**
- **Change supply voltage and/or temperature until OK disappears**
- **Repeat experiment for other operands**

WORKABILITY RANGE



SUMMARY

- Designed speed independent (SI) pipelined 64-bit FMAS unit conforming to IEEE 754 demonstrates high average performance (up to 3.15 Gigaflops), low latency (less than 2 ns), and wide workability range being implemented in 65 nm standard CMOS process
- Developed test environment proves that suggested unit is true SI unit whose functionality does not depend on real parameters of its components
- Next researches will be devoted to decomposition of the multiplier in order to obtain the same performance of the SI-FMAS unit while using one computing channel instead of two identical channels

Thank You!

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