SELF-TIMED STORAGE REGISTER SOFT ERROR TOLERANCE IMPROVEMENT

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OUTLINE

- What is a soft error?
- Self-timed circuits
- Soft error types
- Masking soft error in combinational part and register
- Summary

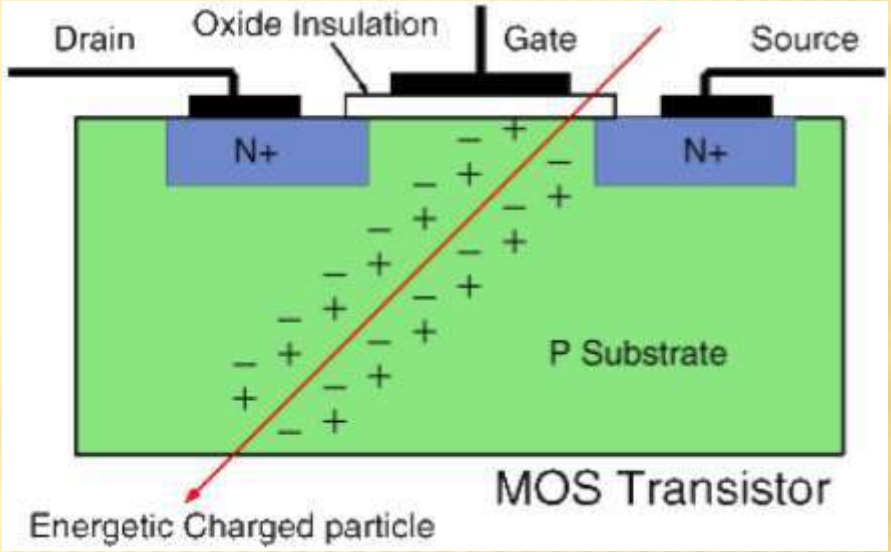
SOFT ERROR PHYSICAL REASONS (1)

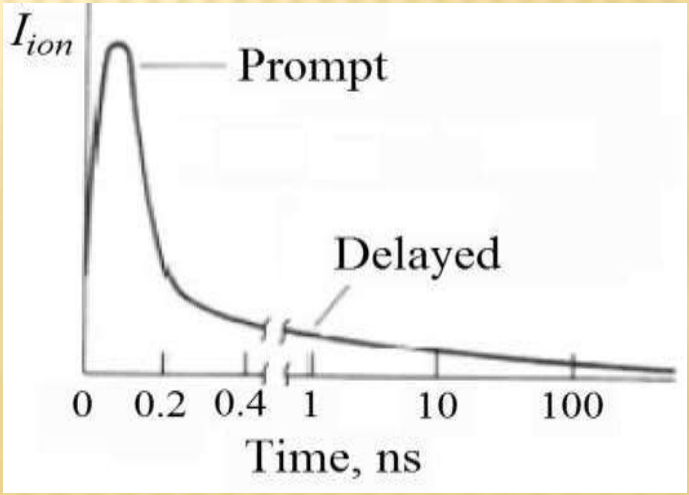
- Cosmic rays
- Radiation
- Nuclear particle

Bulk charge

Ionization current

Short-term pulse

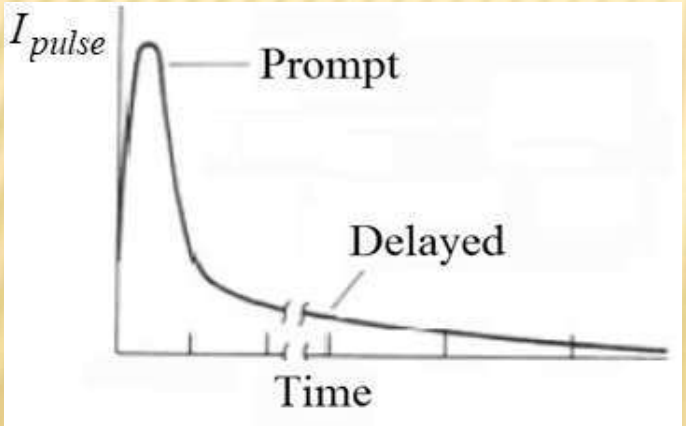


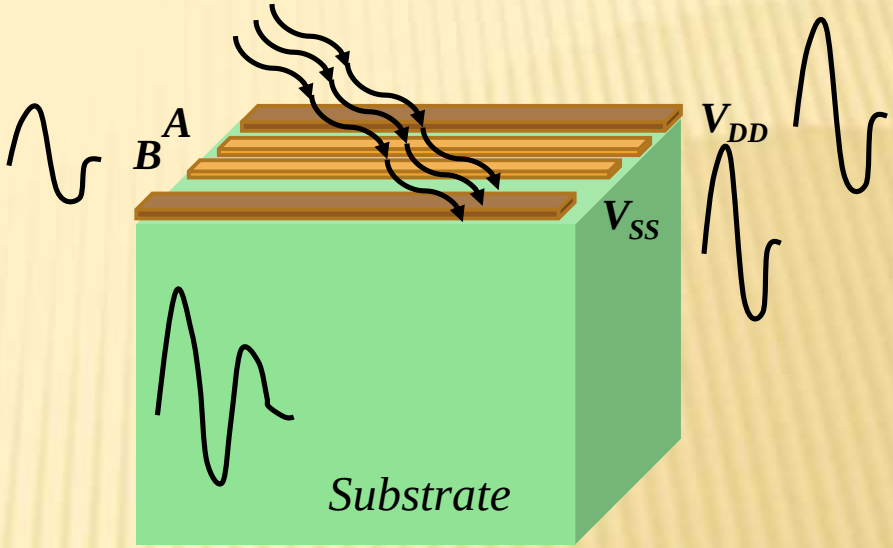


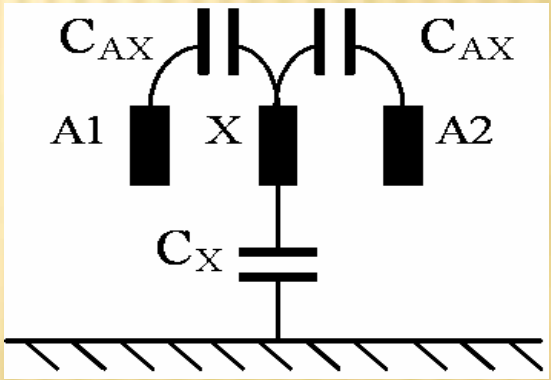
SOFT ERROR PHYSICAL REASONS (2)

- Electromagnetic pulses
- Noise
- Signal cross-talk

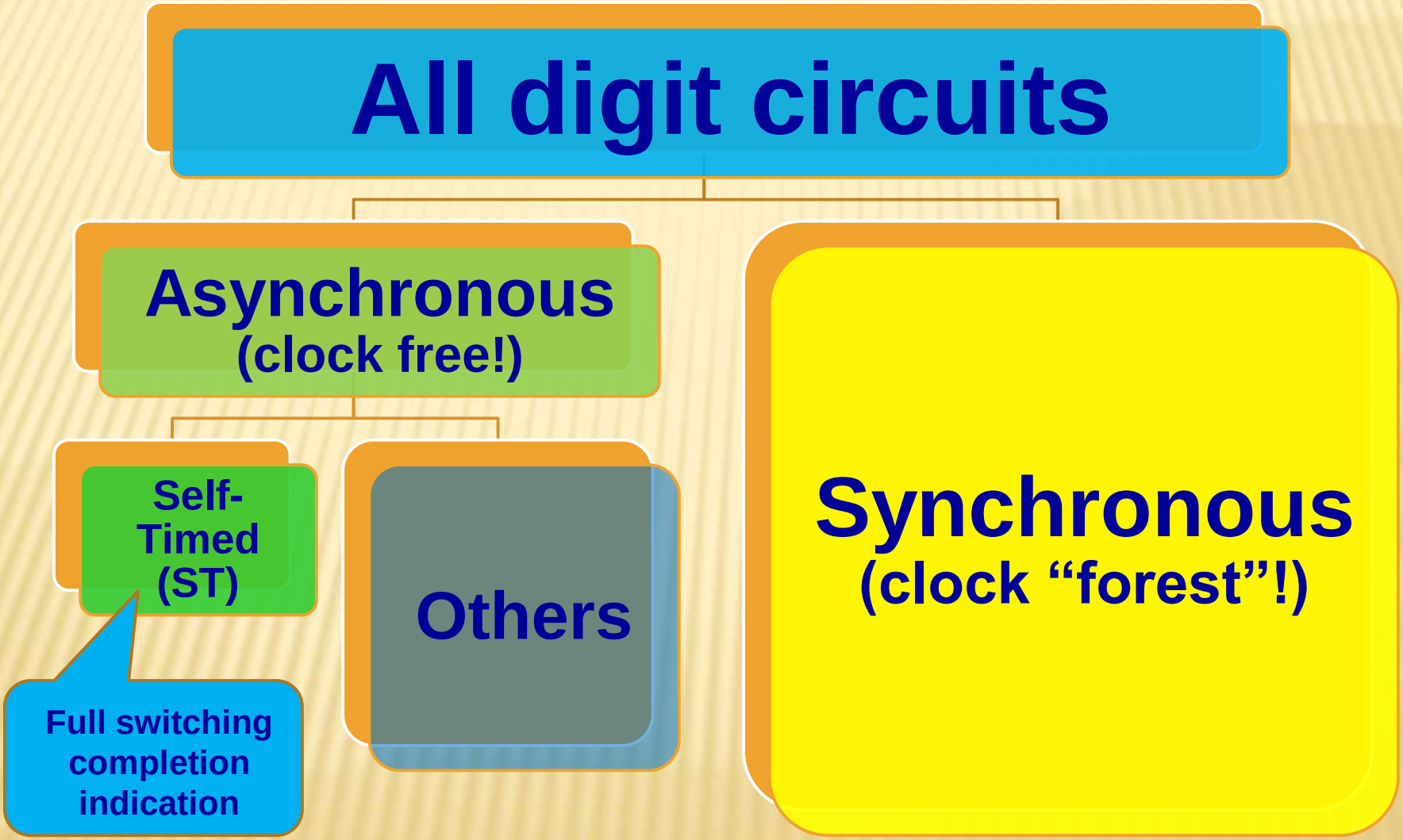
Short-term pulse







CIRCUITS CLASSIFICATION



SELF-TIMED PRINCIPLES

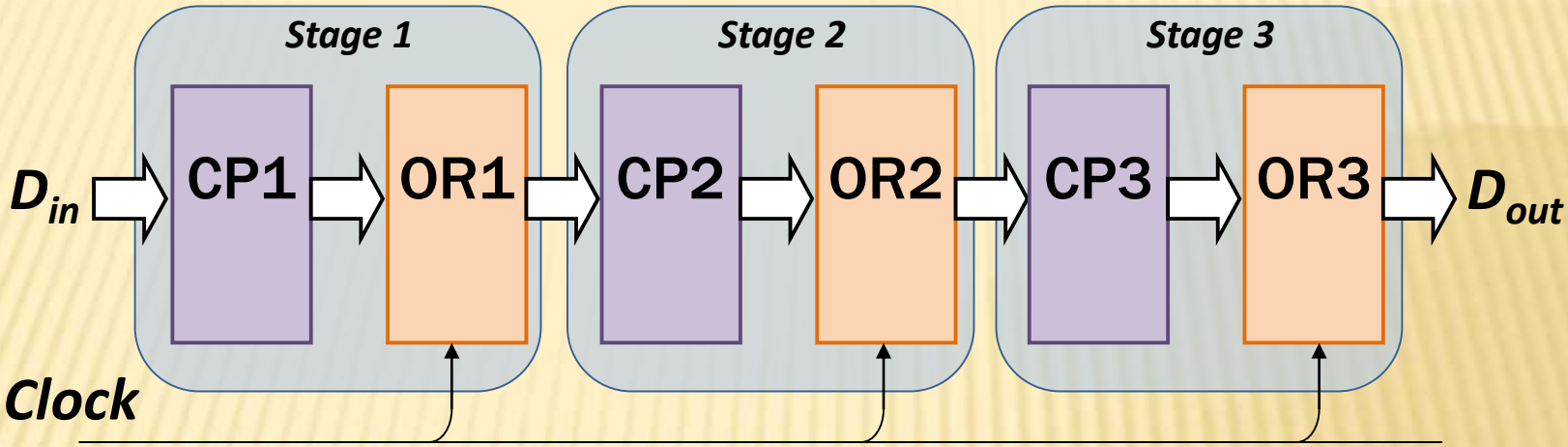
- **Two operation phase:**
  - **work phase (data processing)**
  - **spacer (pause)**
- **Redundant information signal coding (dual-rail)**
- **Full indication of all circuit's cells in each operation phase**

Higher level of soft error tolerance than in synchronous circuits

Soft error tolerance level:

76%

SYNCHRONOUS PIPELINE

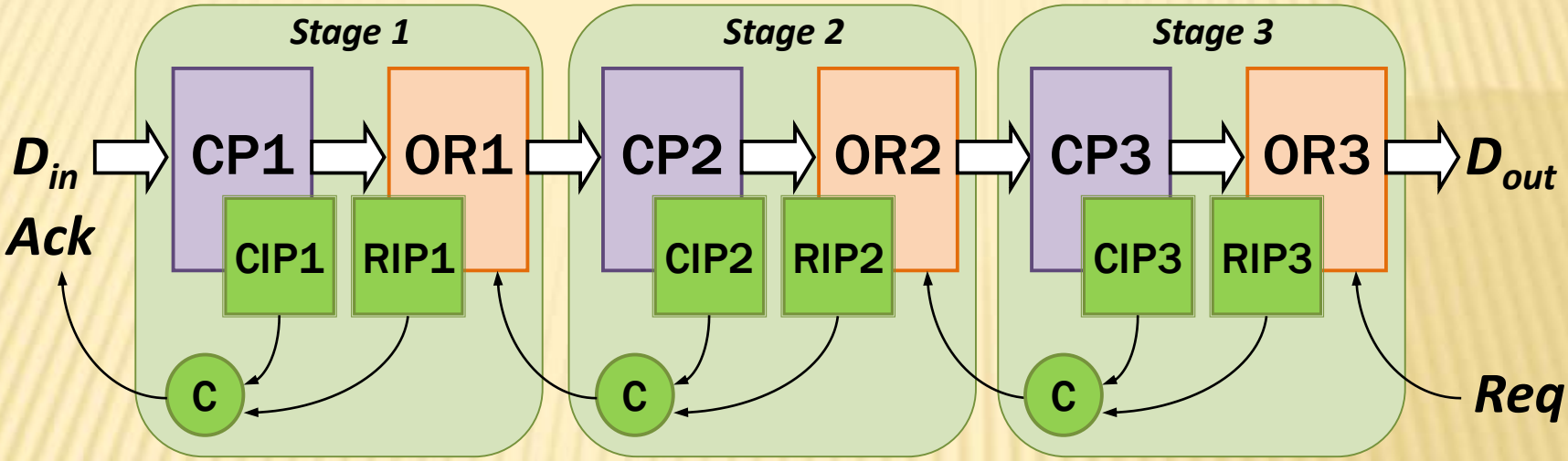


CP – Combinational Part; OR – Output Register

Draw-backs:

- **Worst case performance**
- **Complex clock tree (up to 30% of total power consumption)**

SELF-TIMED PIPELINE

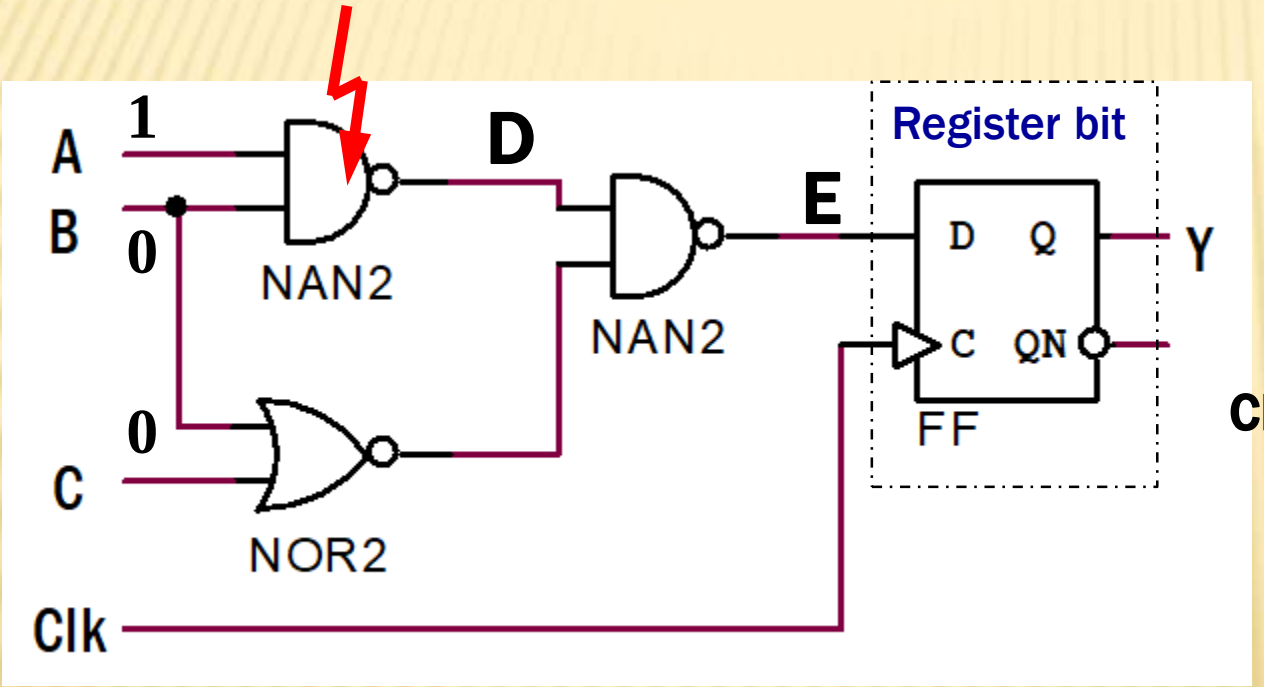


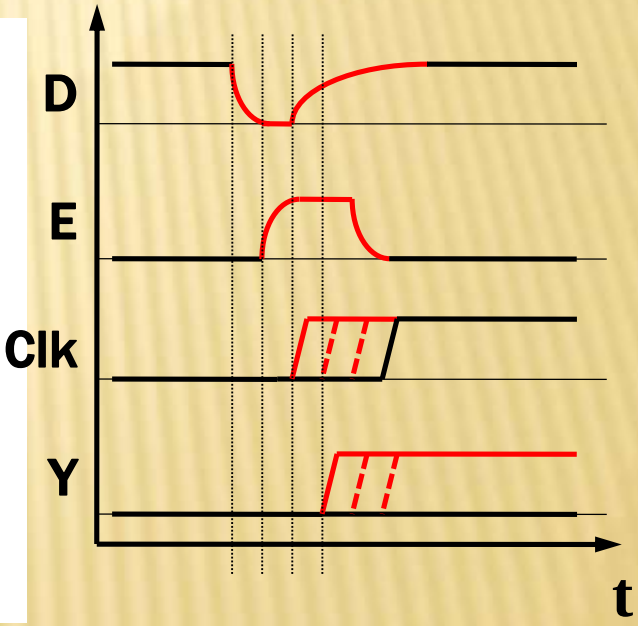
Draw-backs:

- Hardware redundancy (1.5 – 3 times)
- Performance depends on data width

SOFT ERROR IN SYNCHRONOUS CIRCUITS

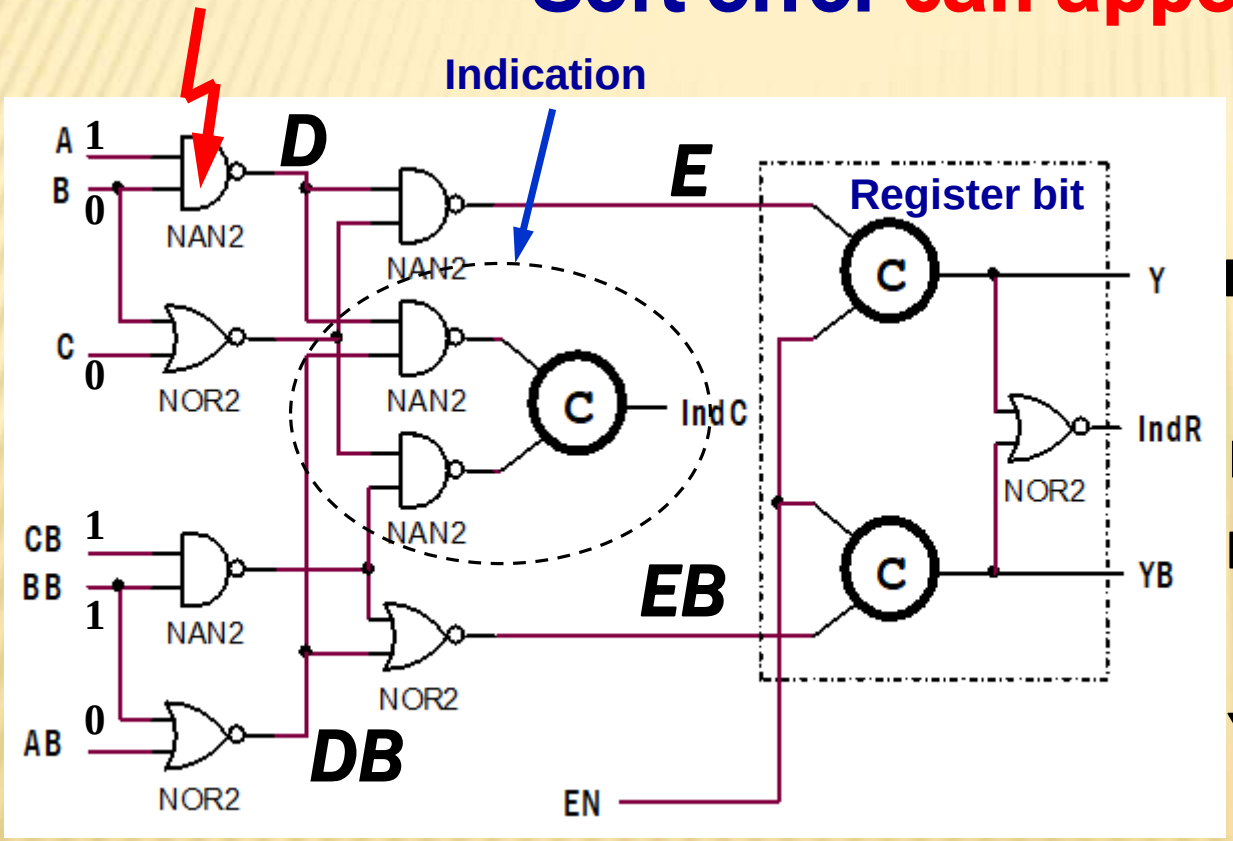
Soft error can appear

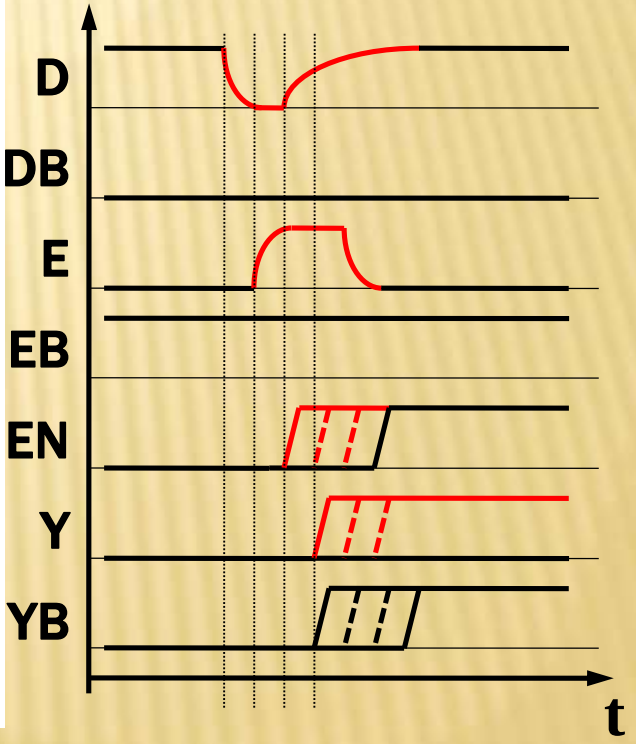




SOFT ERROR IN SELF-TIMED CIRCUITS

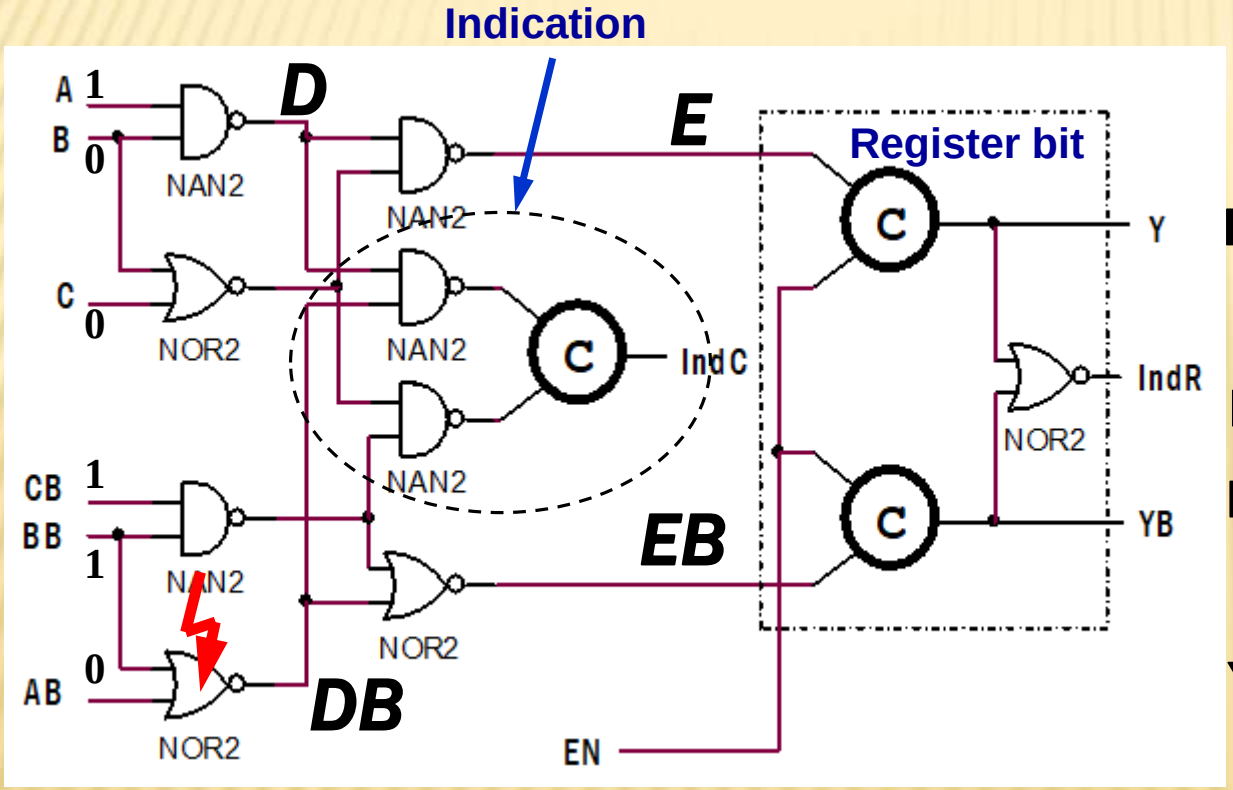
Soft error can appear

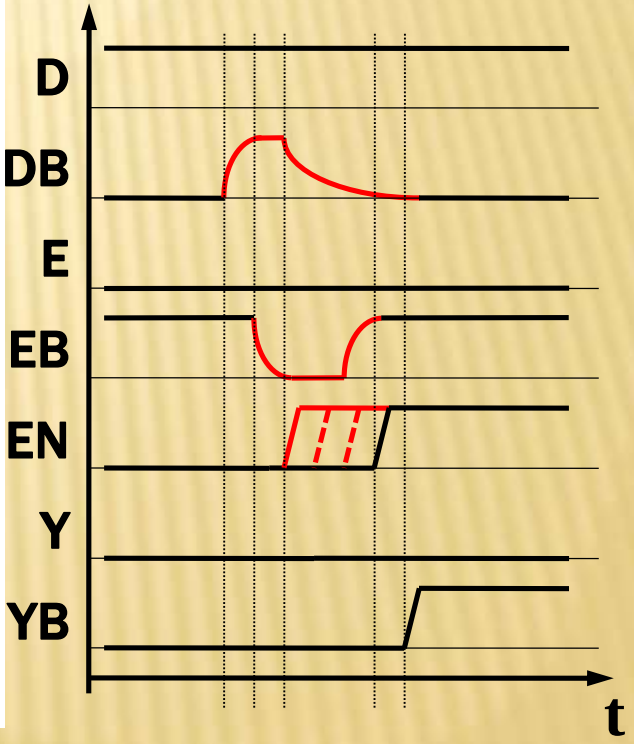




SOFT ERROR IN SELF-TIMED CIRCUITS

Soft error is masked

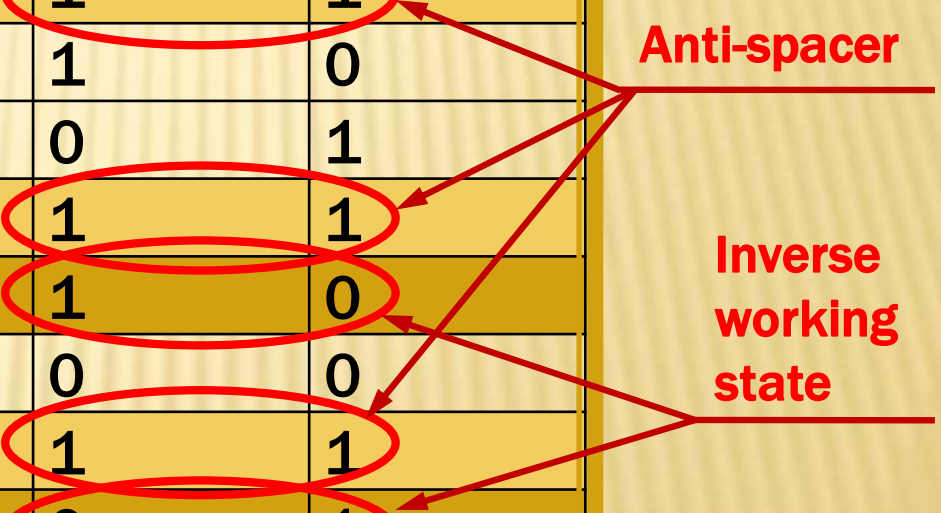




SOFT ERROR TYPES IN ST CIRCUITS

For dual-rail signal (X, XB) with null spacer:

No.	Original state		Faulty state	
	X	*XB*	*X'*	*XB'*
1.	0	0	1	1
2.	0	0	1	0
3.	0	0	0	1
4.	0	1	1	1
5.	0	1	1	0
6.	0	1	0	0
7.	1	0	1	1
8.	1	0	0	1
9.	1	0	0	0



CRITICAL SOFT ERRORS

- **Inverse working state (multiple soft error)**

  One can prevent it by layout techniques:

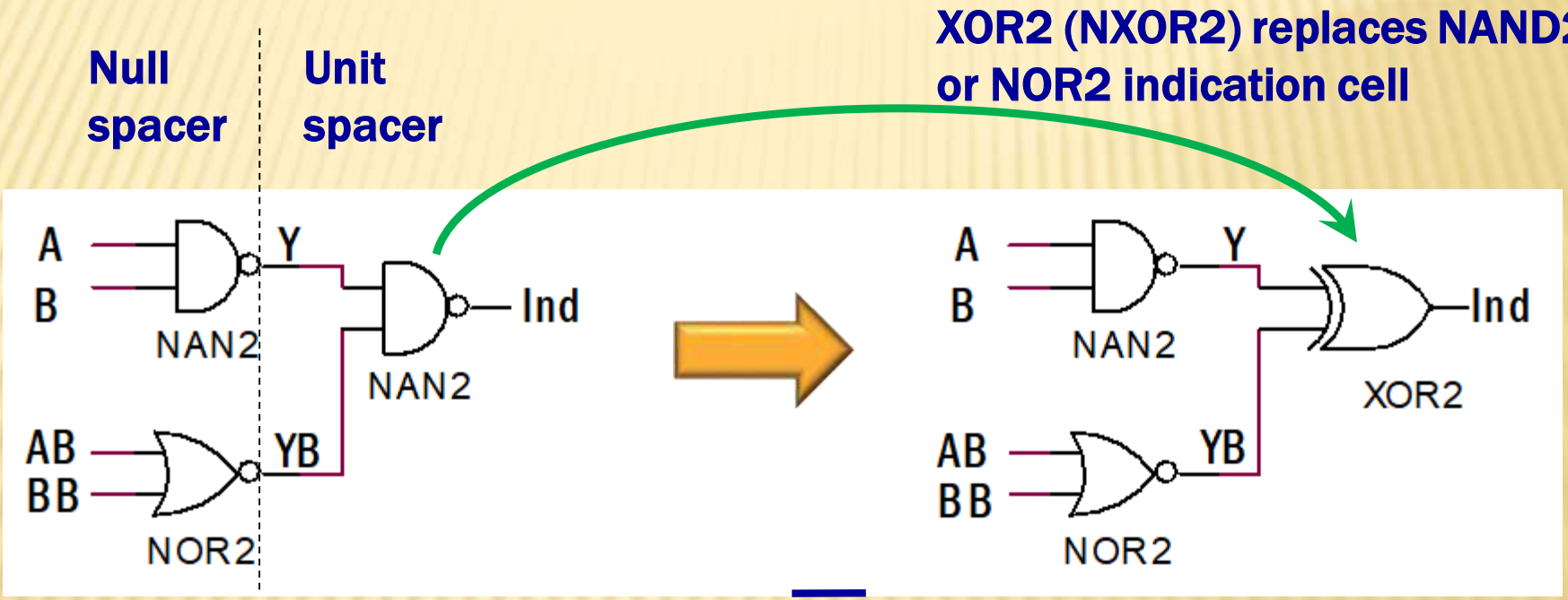
  1) place dual-rail signal components' drivers far enough from each other,
  2) rout dual-rail components' wires close to each other.

- **Anti-spacer (multiple or single soft error)**

  One can mask it by circuitry techniques.

FAILURE TOLERANCE IMPROVEMENT TECHNIQUES (1)

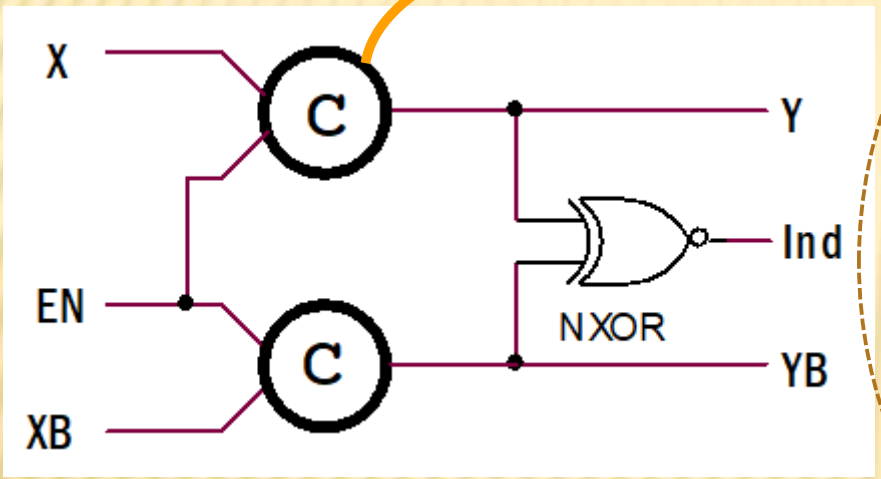
Indicating anti-spacer as spacer



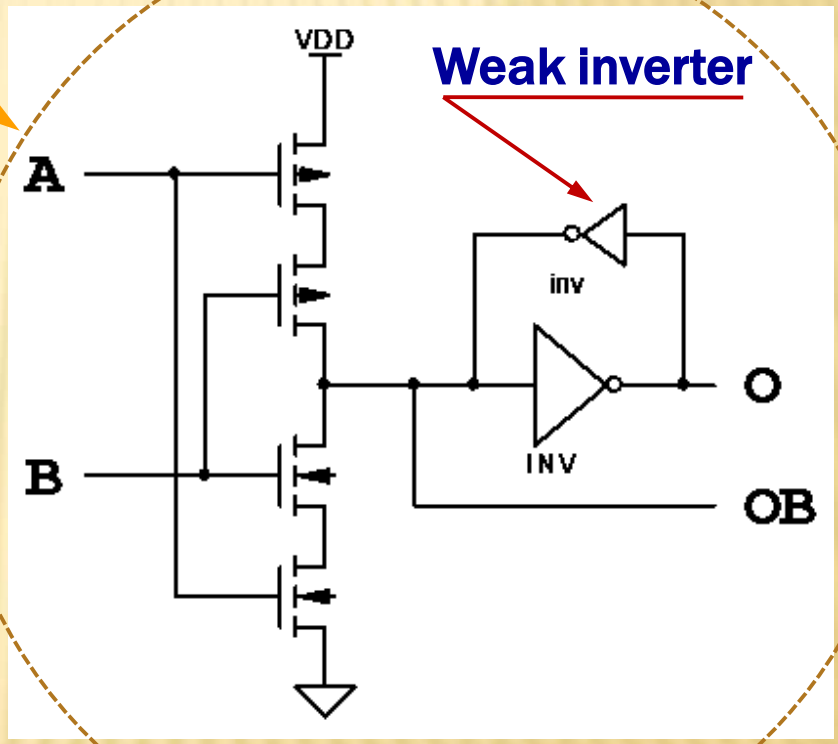
$$Y = \overline{A \cdot B}$$

FAILURE TOLERANCE IMPROVEMENT TECHNIQUES (2)

Register bit



Muller's C-element



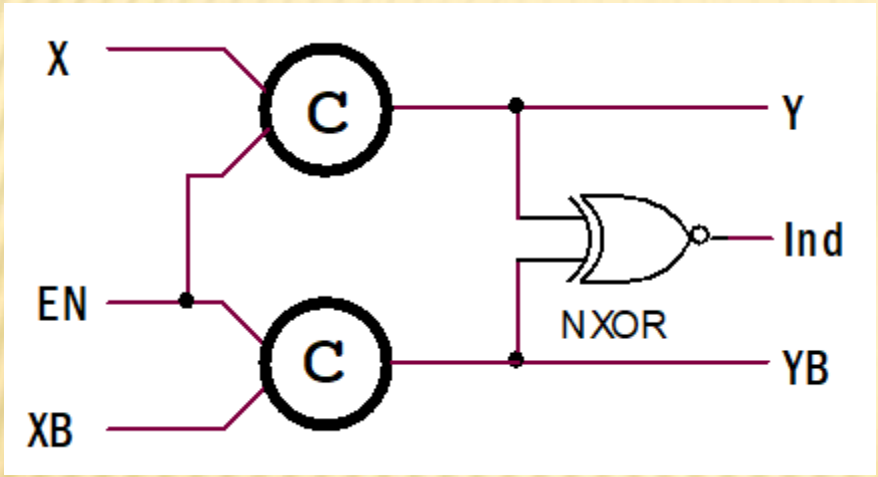
$O^+ = A \cdot B + O \cdot (A + B)$

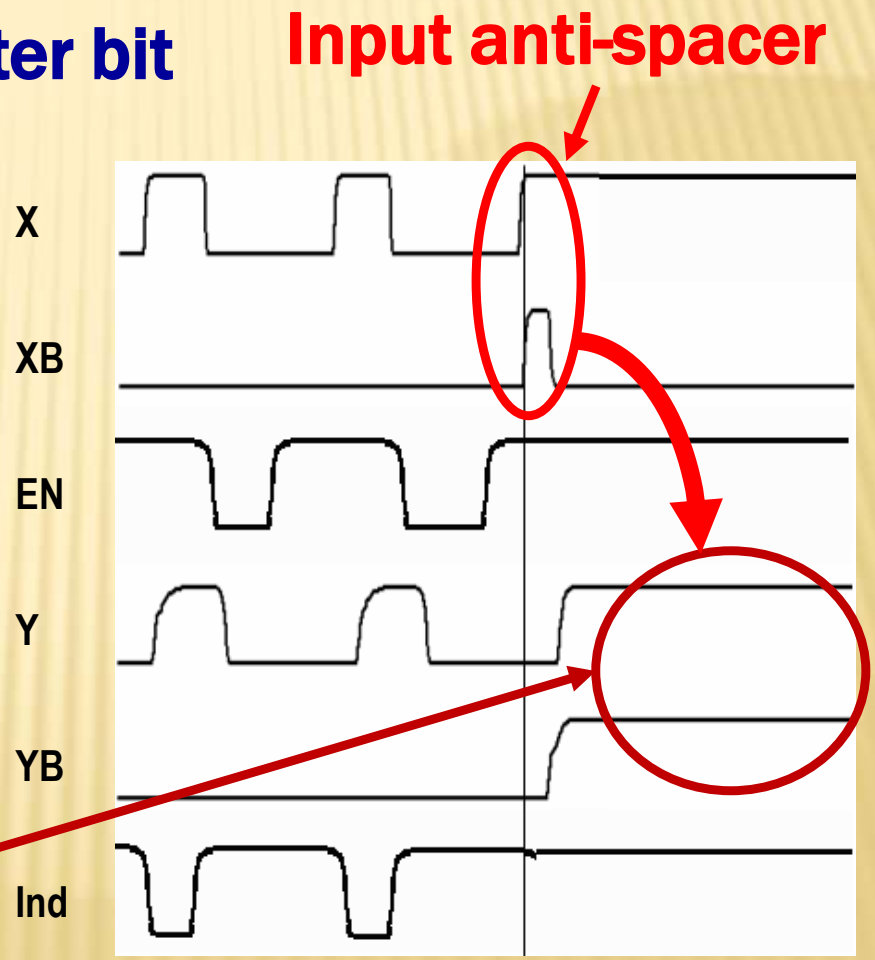
Failure tolerance level

76%

FAILURE TOLERANCE IMPROVEMENT TECHNIQUES (3)

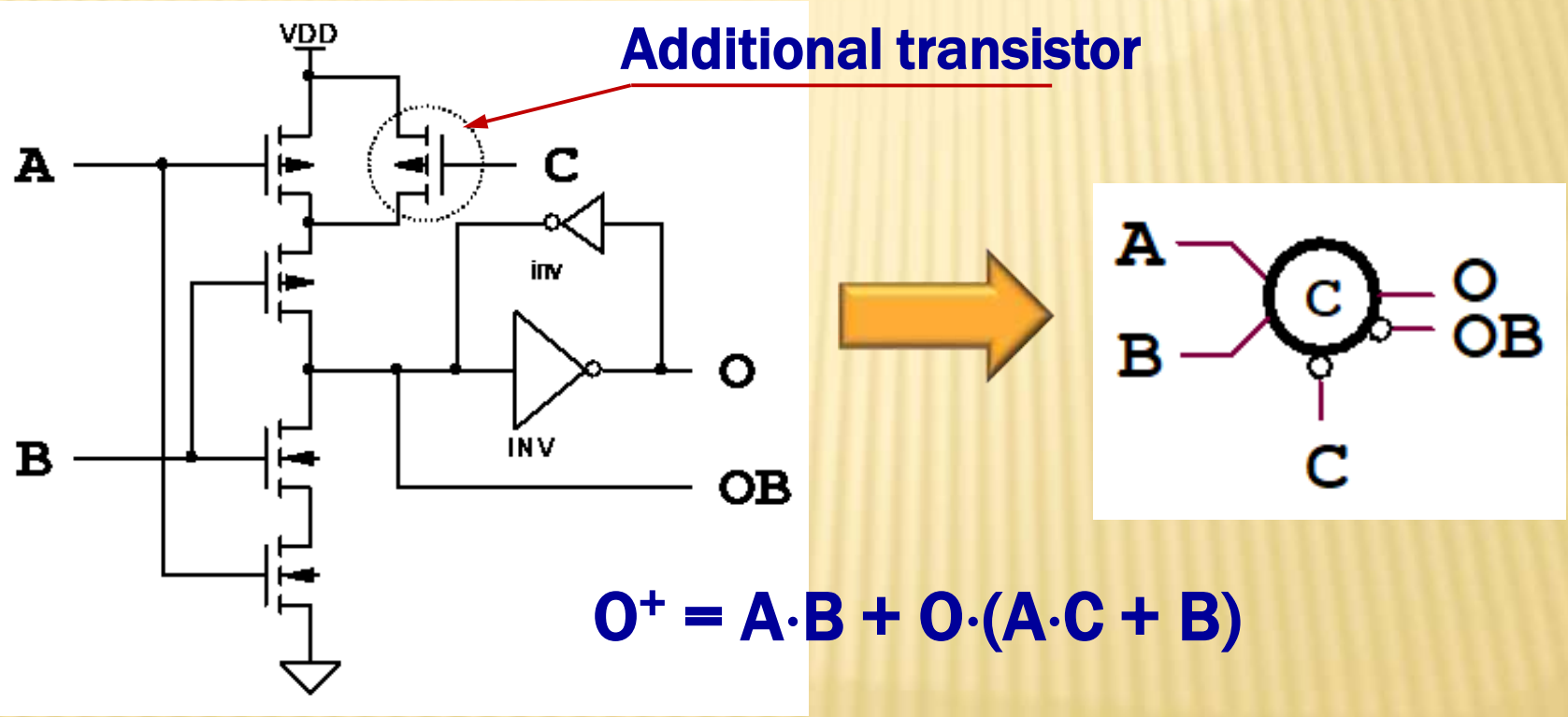
Convenient self-timed register bit





FAILURE TOLERANCE IMPROVEMENT TECHNIQUES (4)

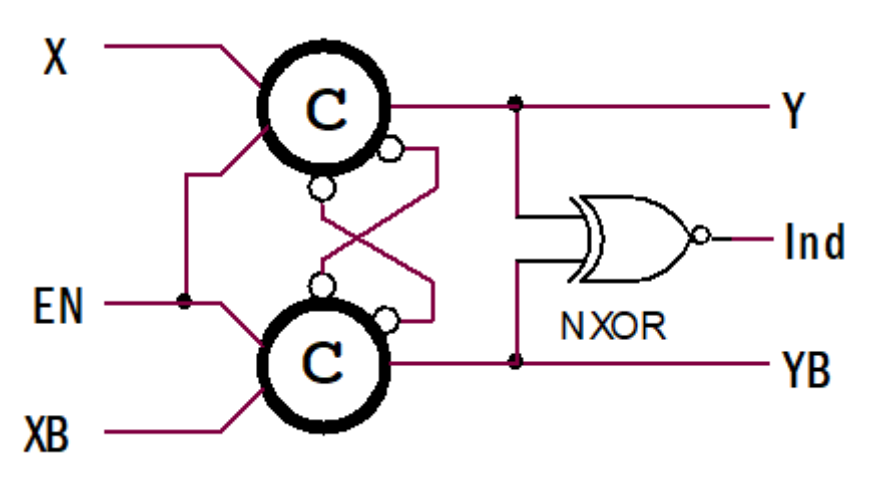
C-element protected against sticking in anti-spacer



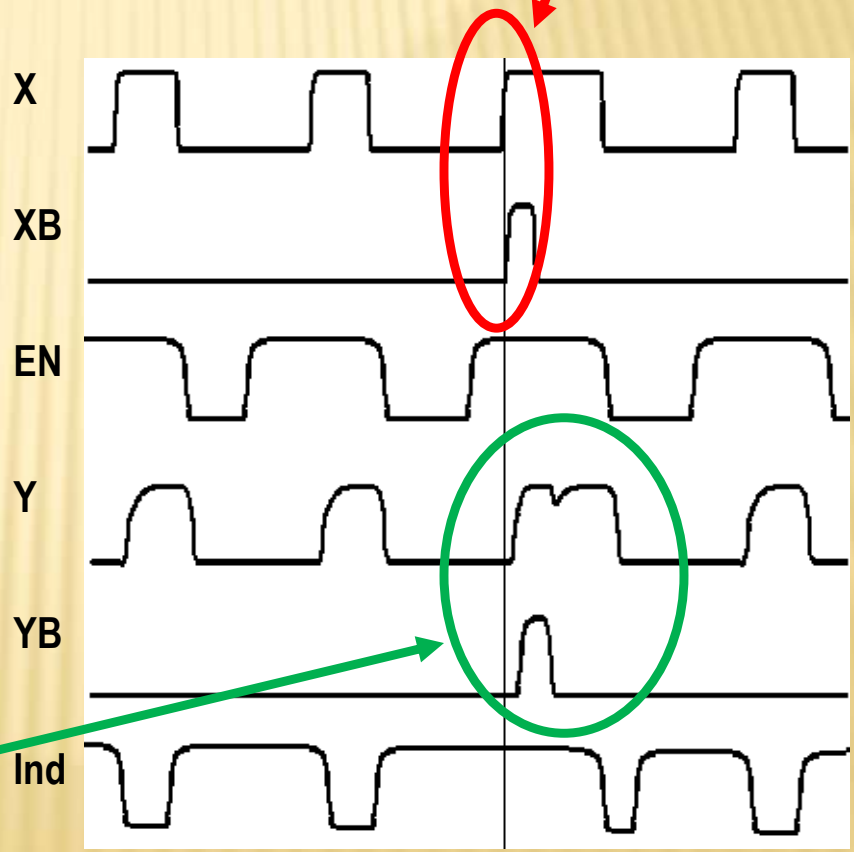
$$O^{+} = A \cdot B + O \cdot (A \cdot C + B)$$

FAILURE TOLERANCE IMPROVEMENT TECHNIQUES (5)

Register bit protected against sticking in anti-spacer state



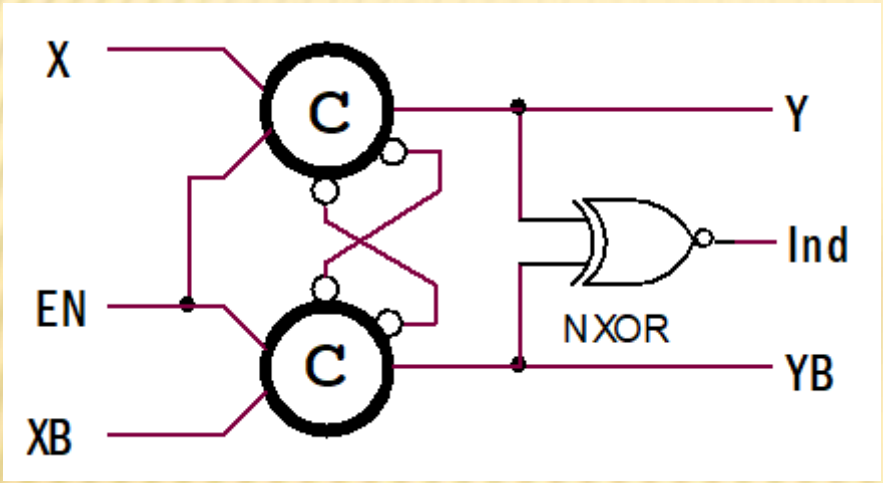
Input anti-spacer



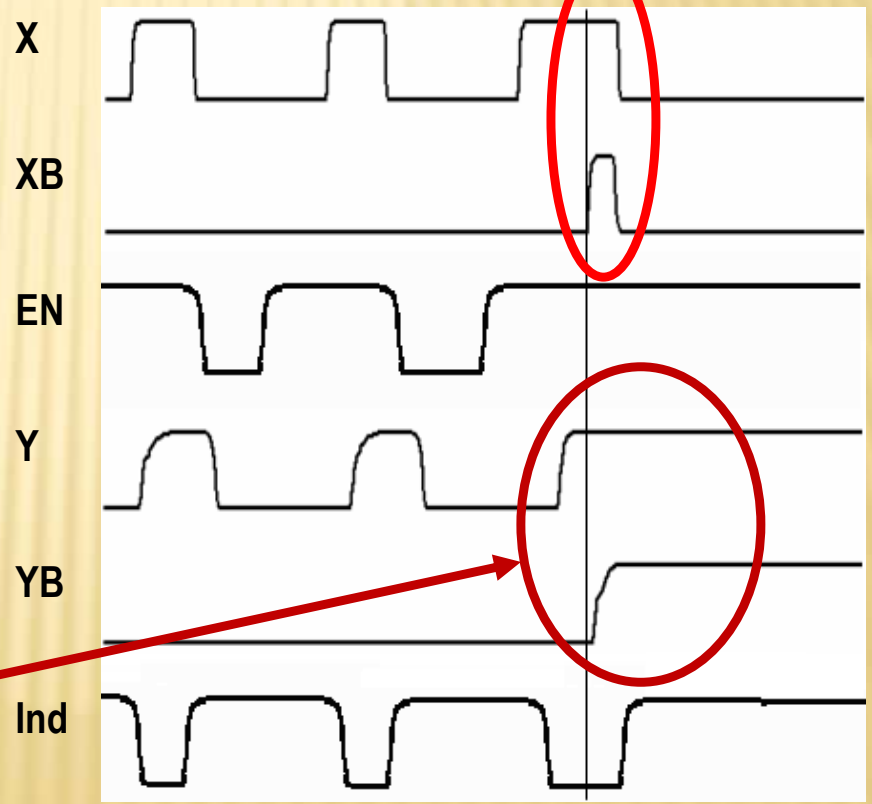
Register bit does not stick in anti-spacer

FAILURE TOLERANCE IMPROVEMENT TECHNIQUES (6)

Not masked anti-spacer case



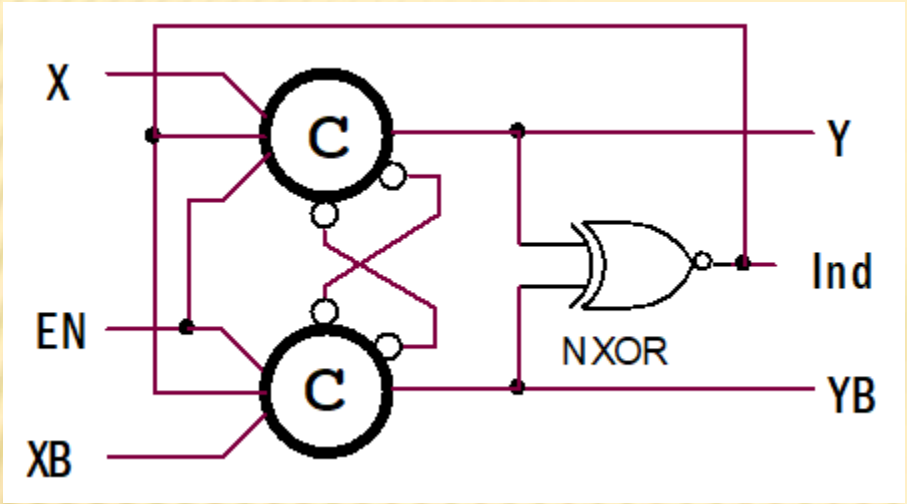
Input anti-spacer



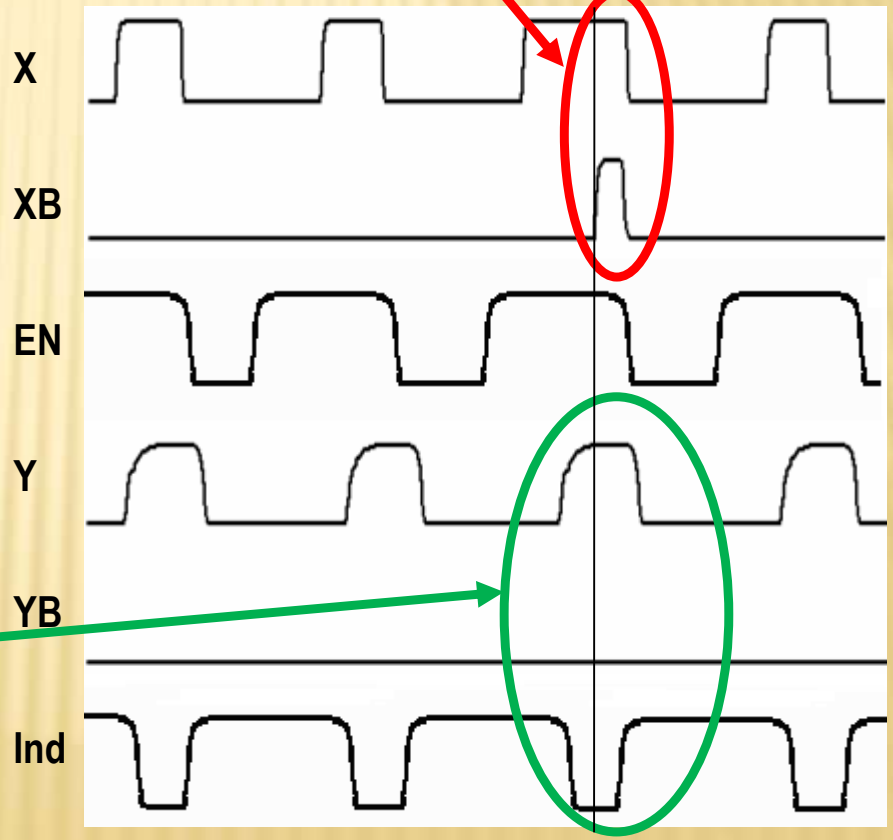
Register bit sticks in anti-spacer

FAILURE TOLERANCE IMPROVEMENT TECHNIQUES (7)

Resilient register bit



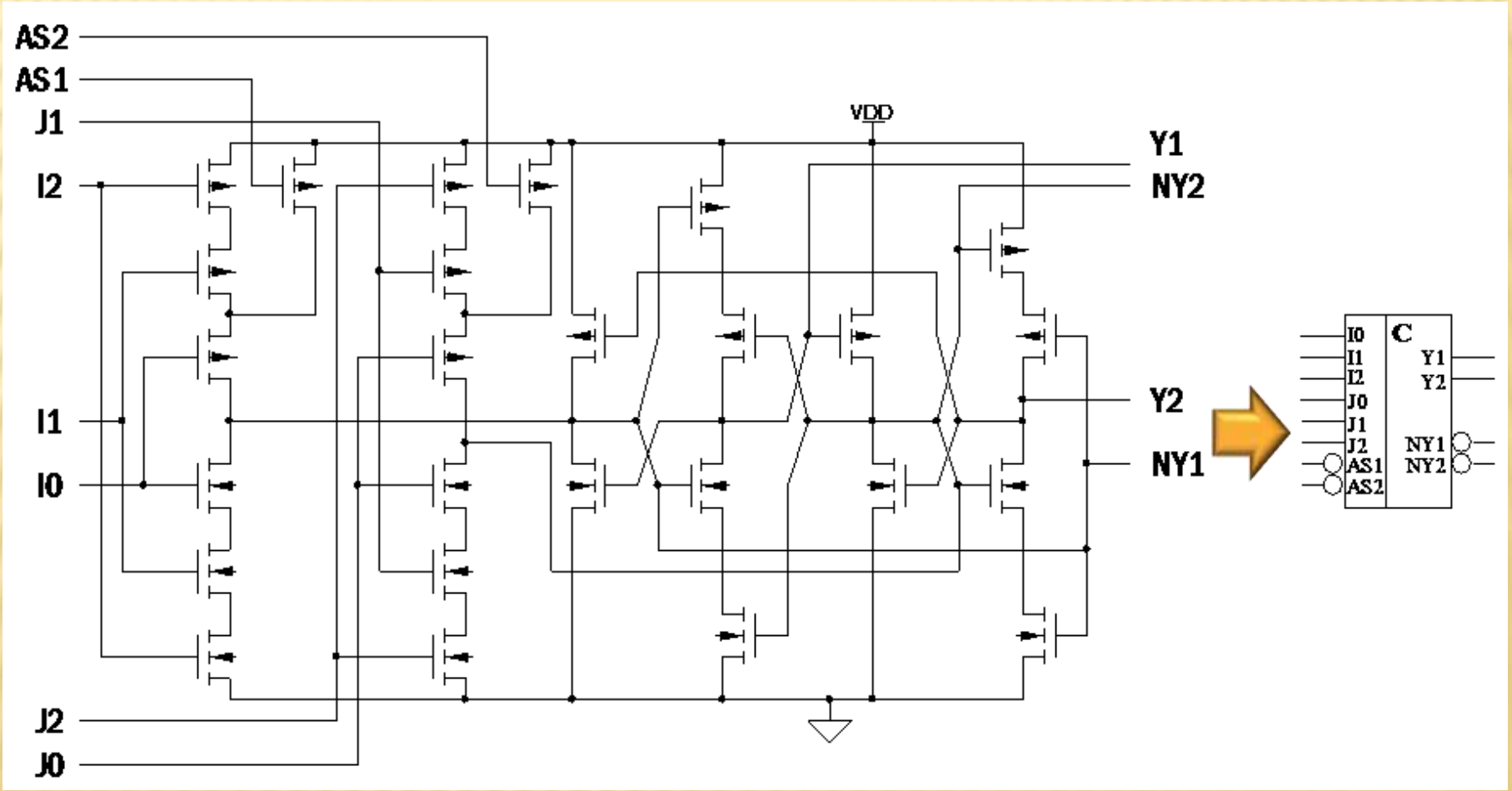
Input anti-spacer



Feedback from output "Ind" protects writen correct state against switching to the anti-spacer

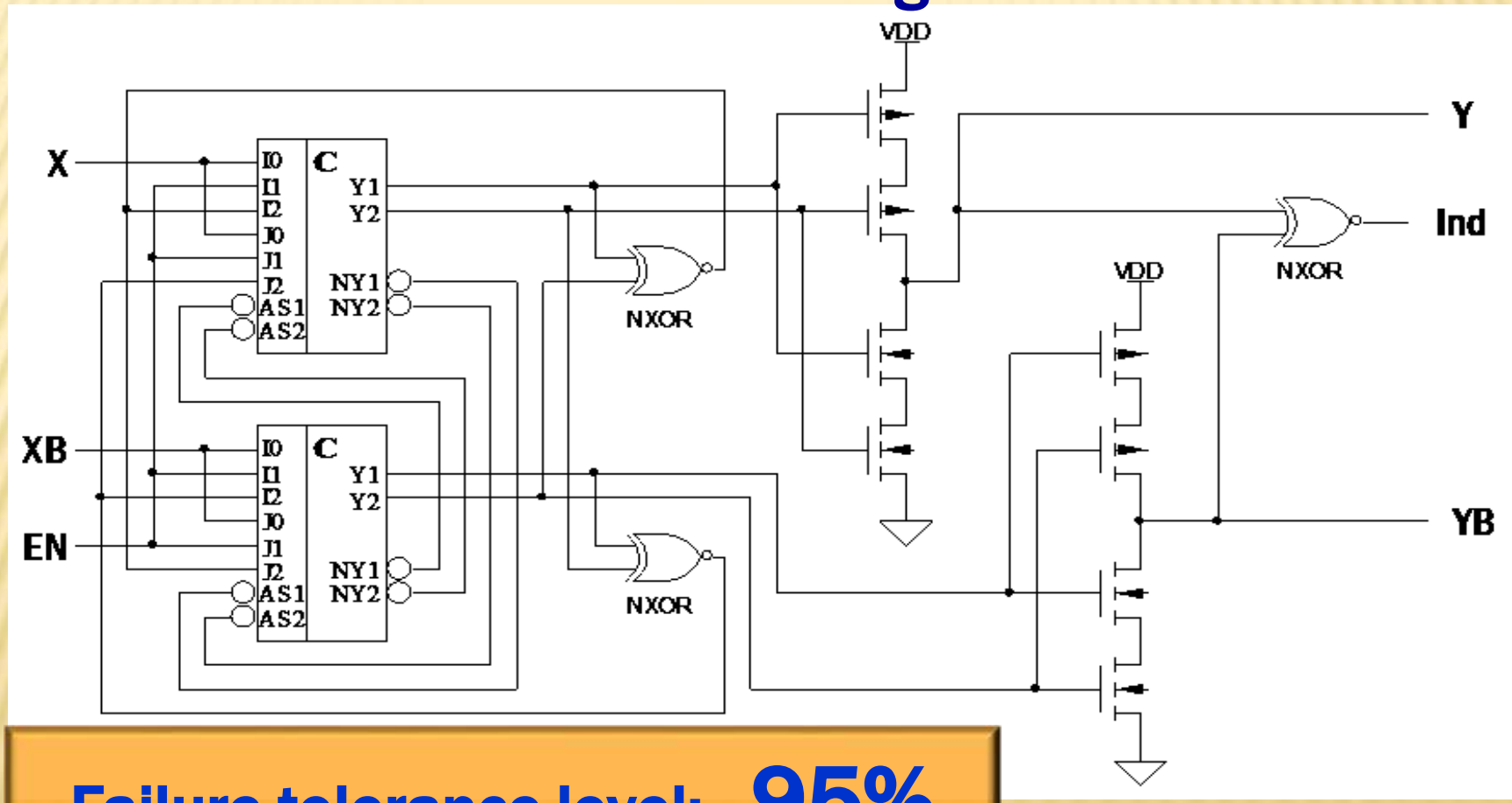
FAILURE TOLERANCE IMPROVEMENT TECHNIQUES (8)

DICE-like C-element masks any inside soft error



FAILURE TOLERANCE IMPROVEMENT TECHNIQUES (9)

DICE-like fail-safe register bit



Failure tolerance level: 95%

SUMMARY

- The proposed layout techniques reduce the number of soft error types in ST circuits
- The circuitry techniques, including cross-connections and local feedback, prevent the ST pipeline register from sticking in the anti-spacer state
- The use of a DICE-like C-element ensures the register bit's immunity to soft errors inside it
- All proposed techniques improve the ST circuit’s soft error tolerance level from 76% to 95%

CONTACTS

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