Improvement of Self-Timed Pipeline's Immunity of Soft Errors

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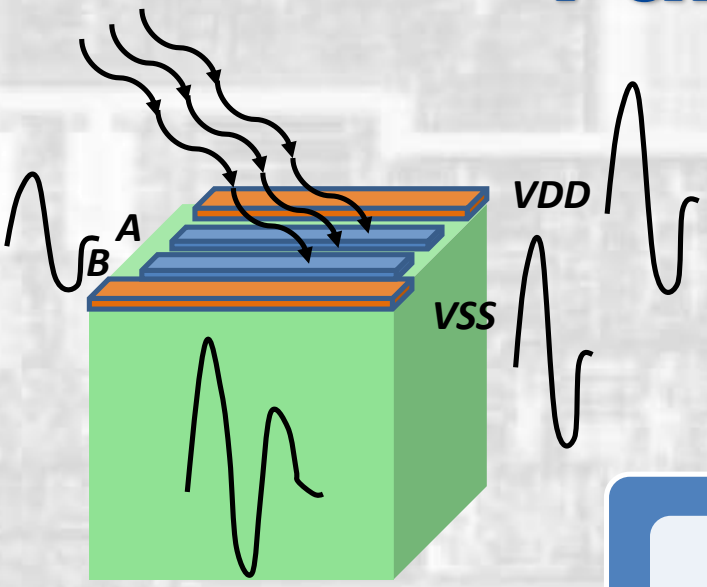
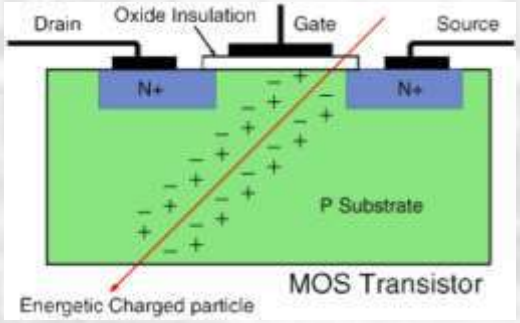
Content

- Reasons for digital circuits' failures
- Self-timed circuit features
- Self-timed pipeline structure
- Self-timed pipeline's failure tolerance
- Improvement of the self-timed pipeline's tolerance
  - Combinational part
  - Register
  - Indication subcircuit
- Conclusions

Failure Types



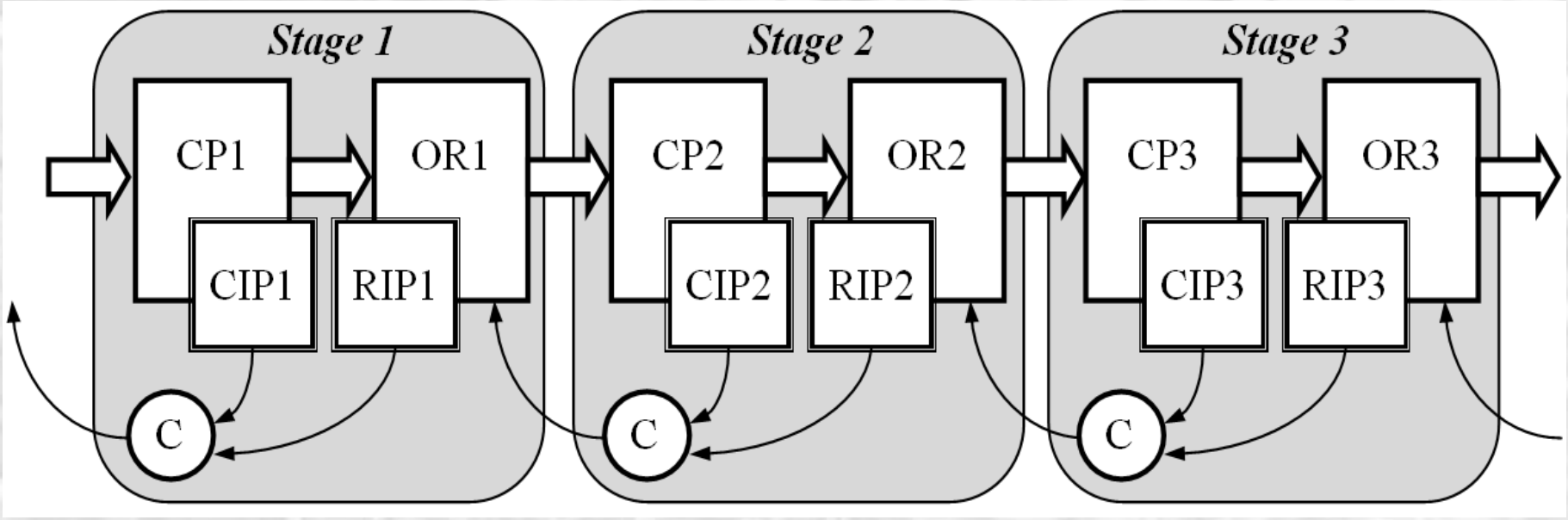


- Failure
  - Soft error
    - Self-disappeared
    - Critical
  - Fault

Self-Timed Circuit's Features

- An absence of a global clock tree,
- The logic cells' delays determine their performance in any operating conditions,
- Two-phase operation mode and a request-acknowledge interaction based on indication signals confirming the completion of circuit switching,
- Less sensitivity to soft error than their synchronous counterparts,
- Complete constant failures self-checking.

Self-Timed Pipeline

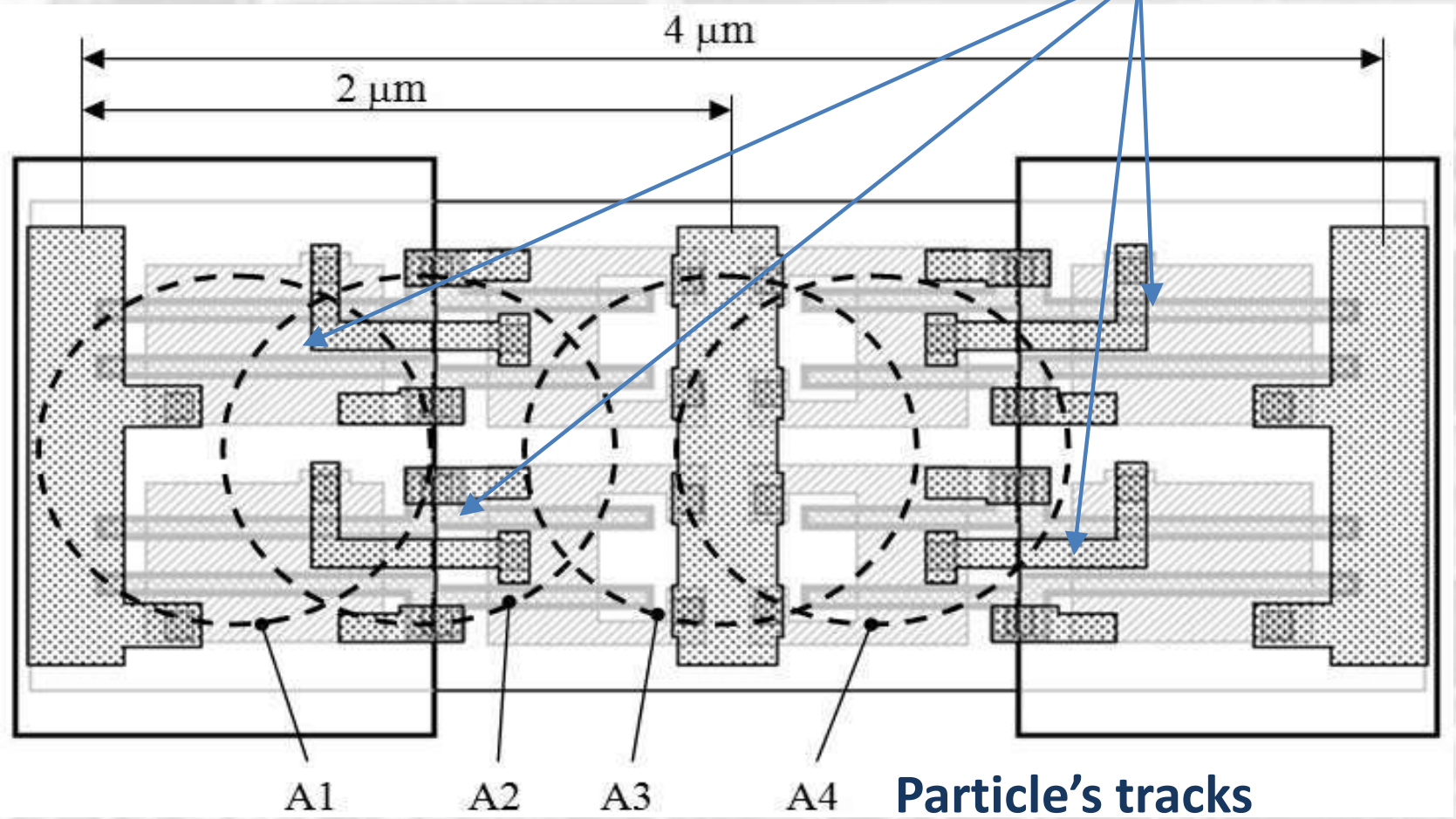


- CP – Combinational Part
- OR – Output Register
- CIP – Combinational Indication Part
- RIP – Register Indication Part

Dual-Rail Coding With Null Spacer

Coded state	X	XB	Phase
Bit “0”	0	1	Working
Bit “1”	1	0	Working
Spacer	0	0	Spacer
Anti-spacer	1	1	Forbidden

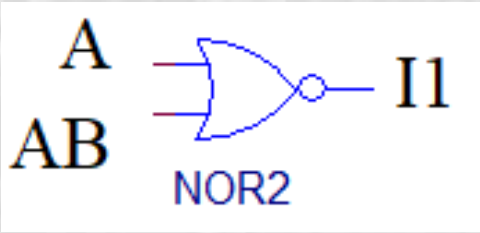
Nuclear Particle Impact



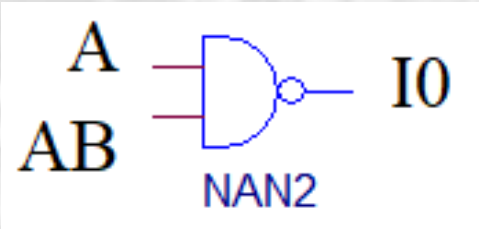
Dual-Rail Signal Indication

XOR2 and XNOR2 mask anti-spacer

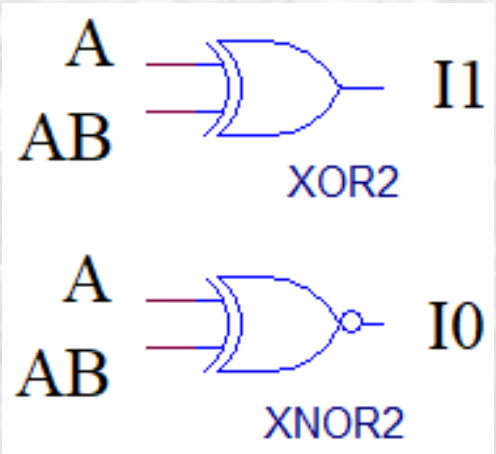
Null input spacer



Unit input spacer



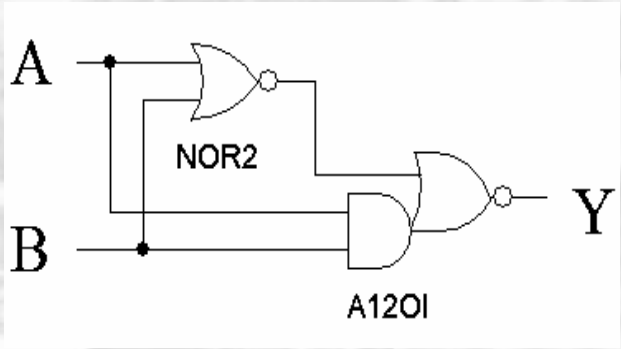
Any input spacer



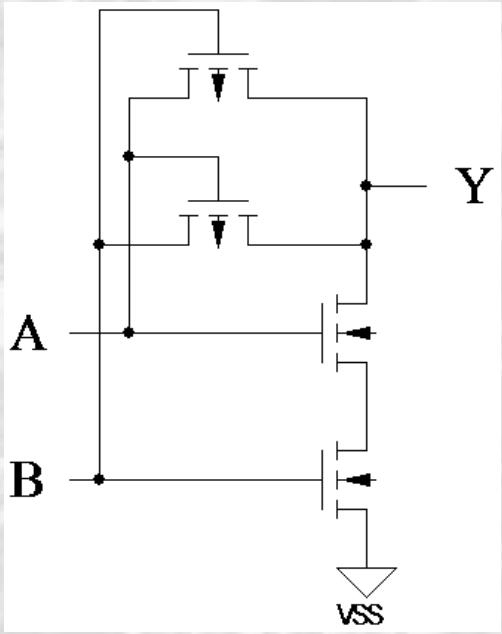
Self-Timed XOR2 Implementations

$$Y = A \oplus B$$

Standard cells



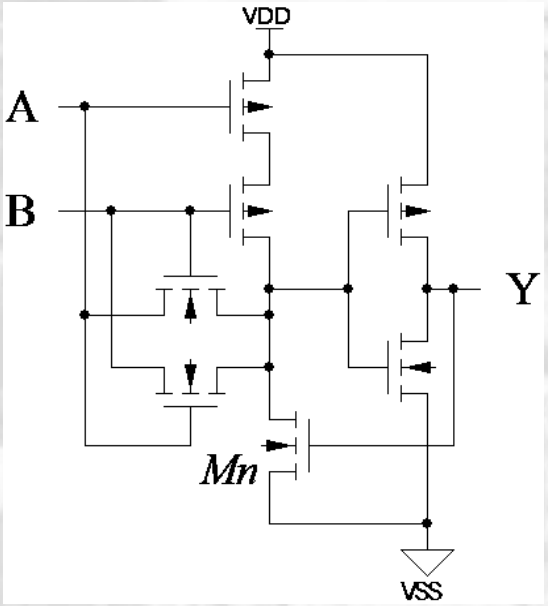
CMOS transistors



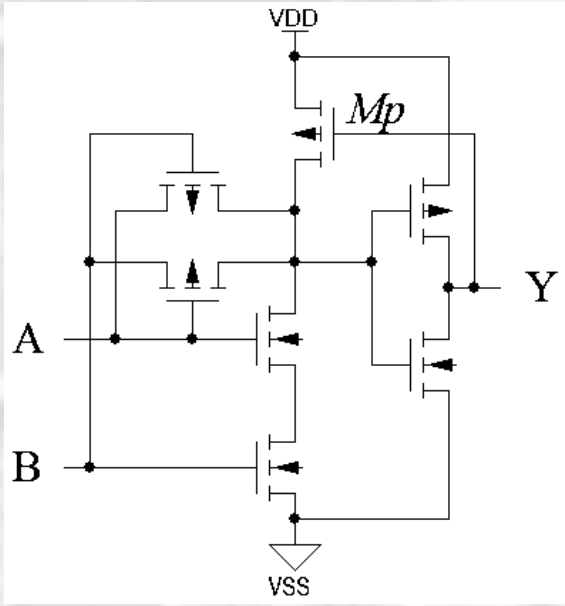
$$V(Y) = V_{th.p} \text{ at } A = B = 0$$

Self-Timed XOR2 and XNOR2

$Y = A \oplus B$



$Y = \overline{A \oplus B}$

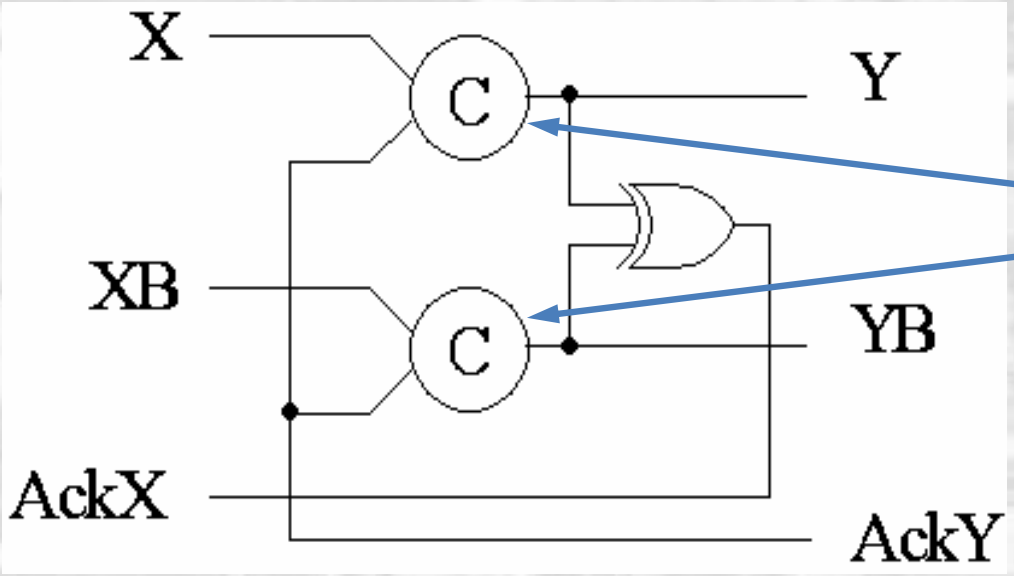


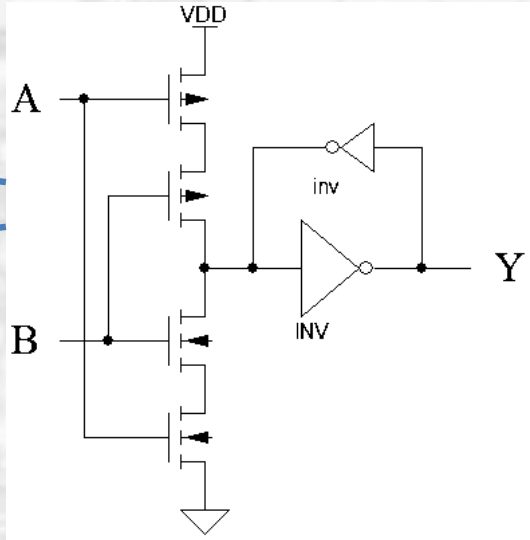
***Mn* and *Mp* transistors repair logical levels**

ST pipeline's combinational part tolerance:

72% → 98%

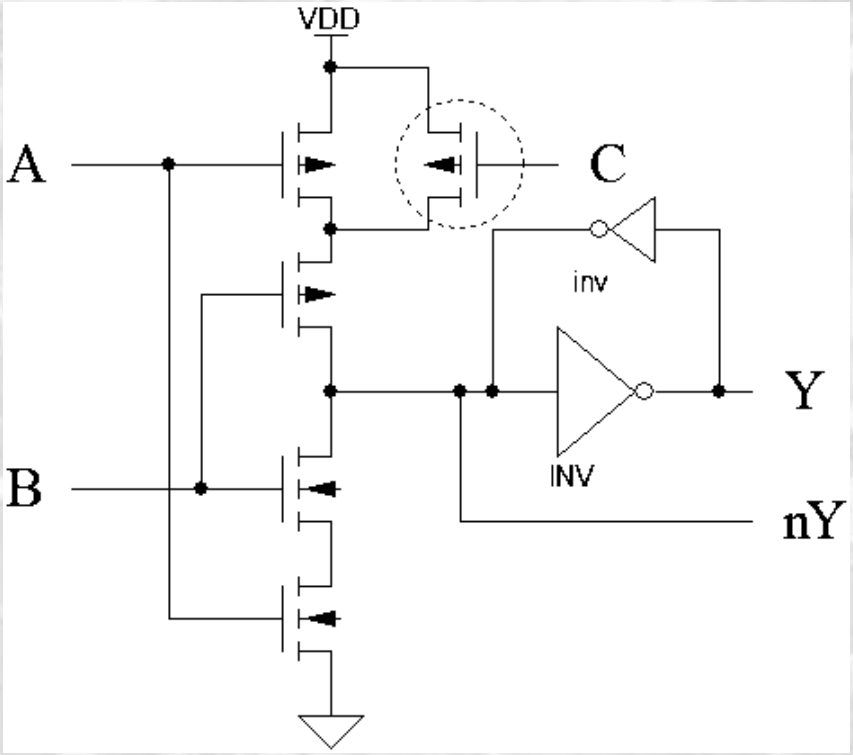
ST Pipeline's Register Bit

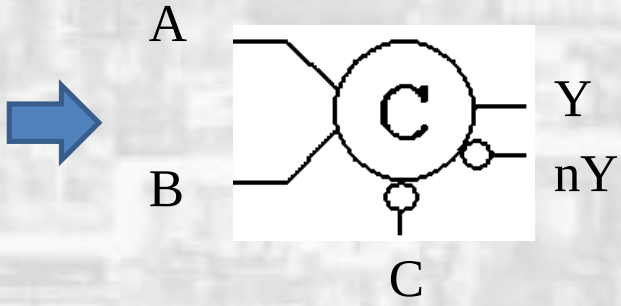




- **Dual-rail input (X, XB) and output (Y, YB)**
- **Stores both working state and spacer**
- **Indication cell XOR**
- **Minimal complexity**

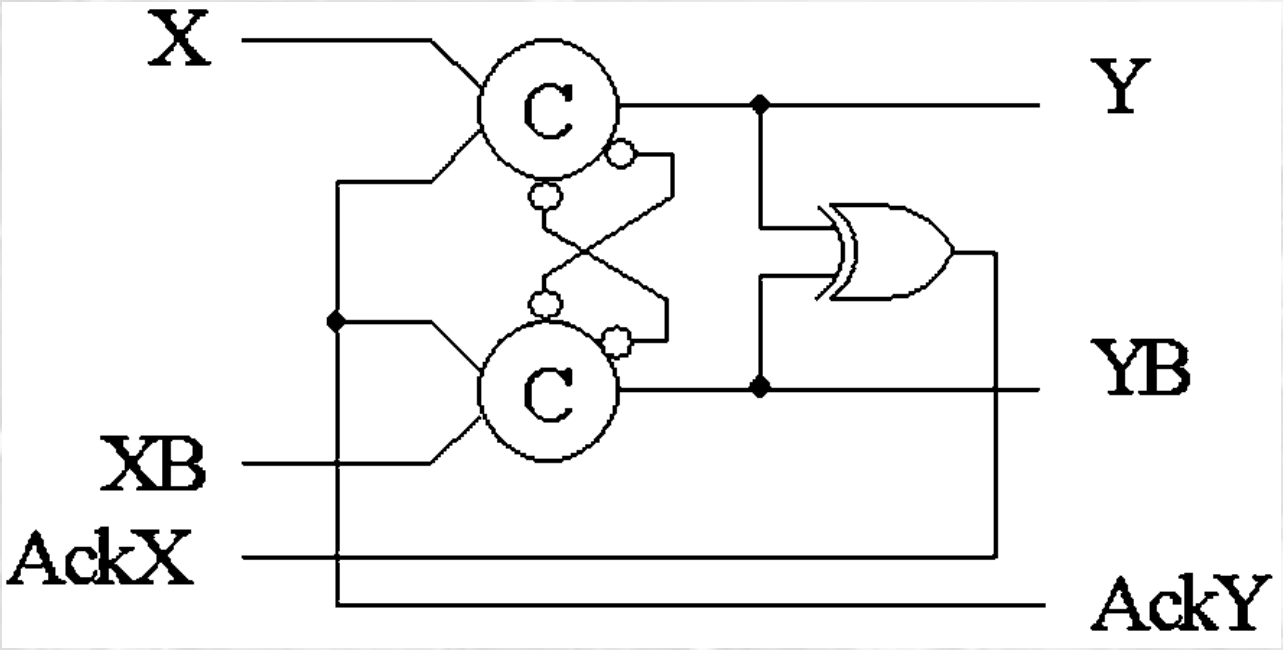
Improved C-element





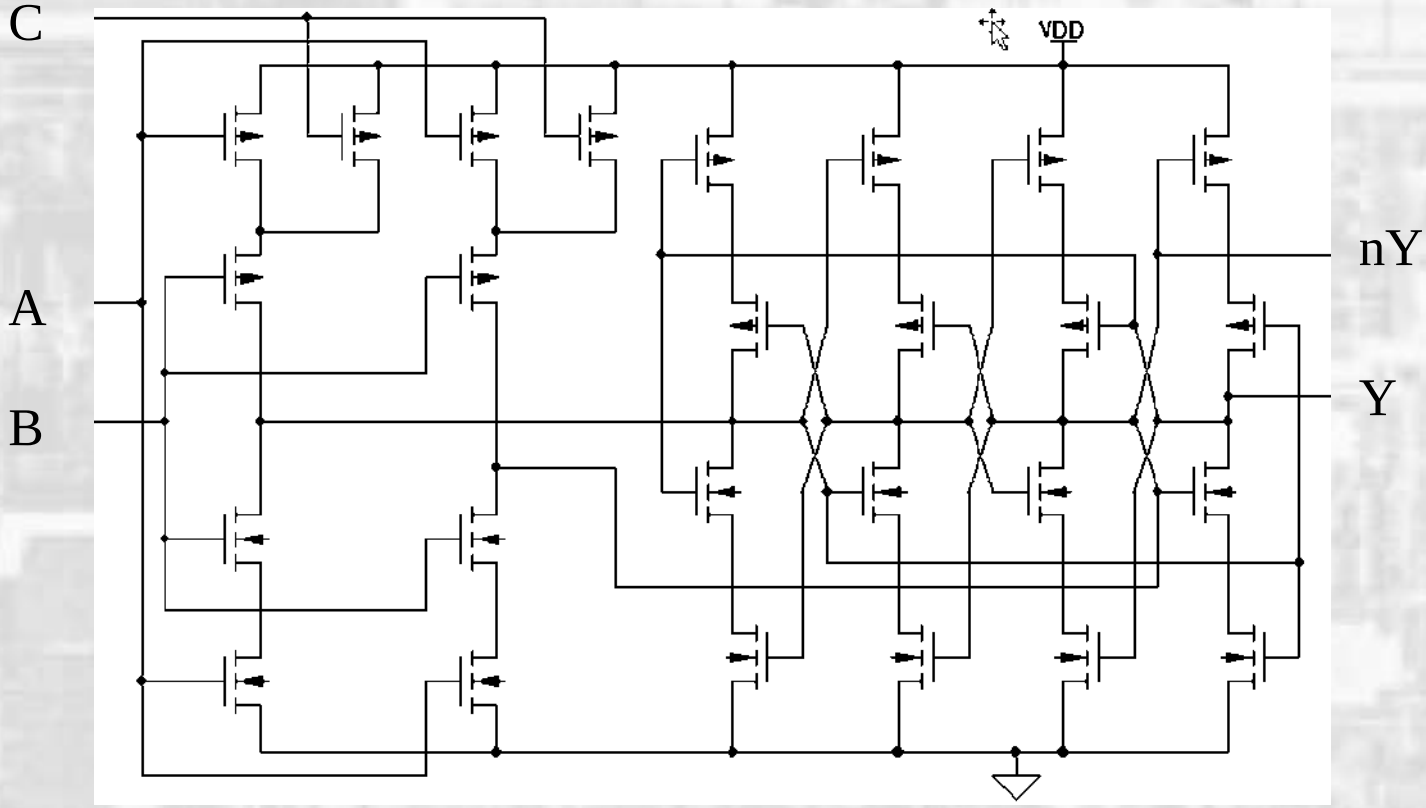
Input “C” prevents sticking in anti-spacer state Y=1

Improved Register Bit



Improved C-elements and cross-feedbacks prevent sticking in anti-spacer state Y=YB=1

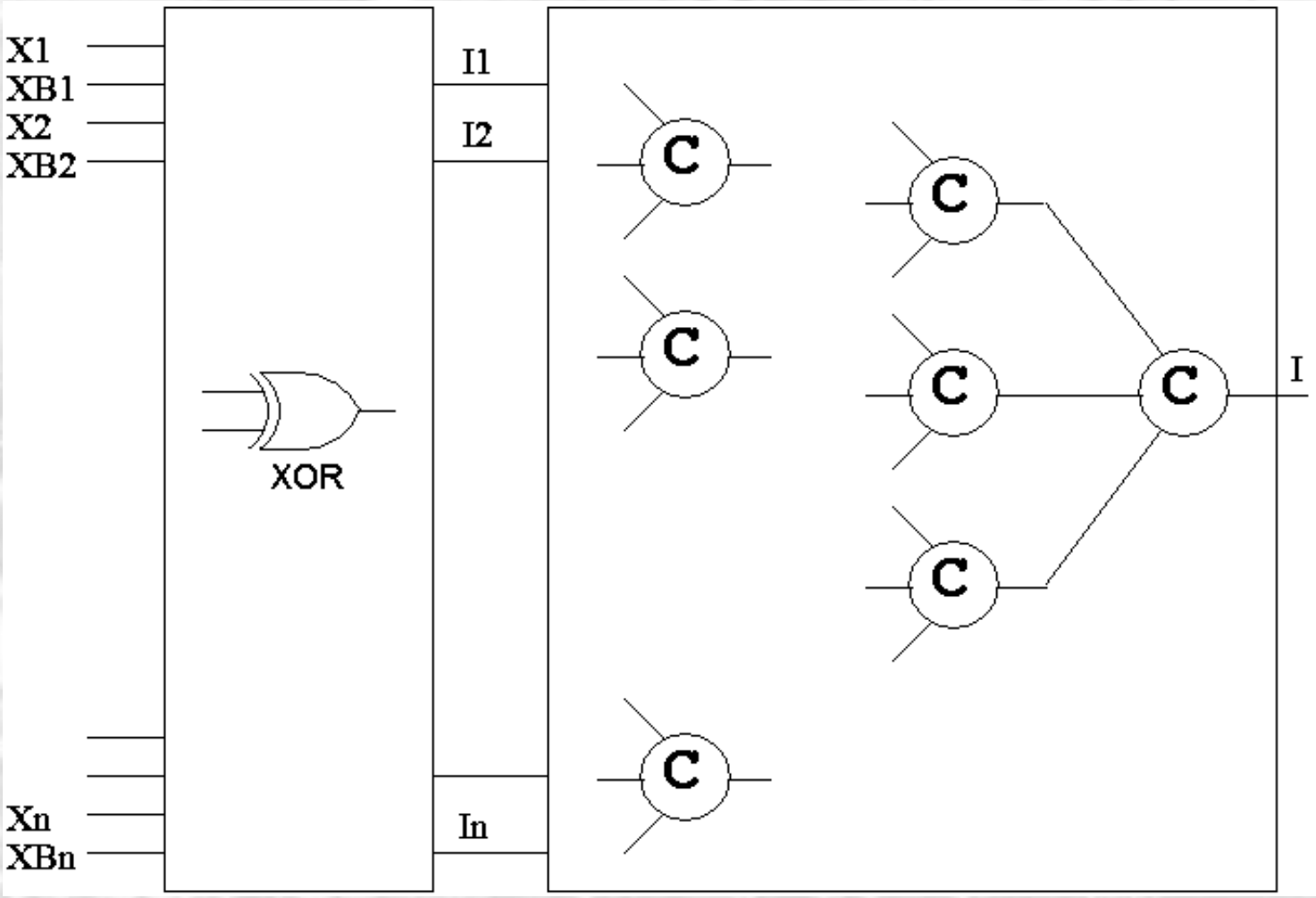
Dual Interlocked Cell (DICE) C-element



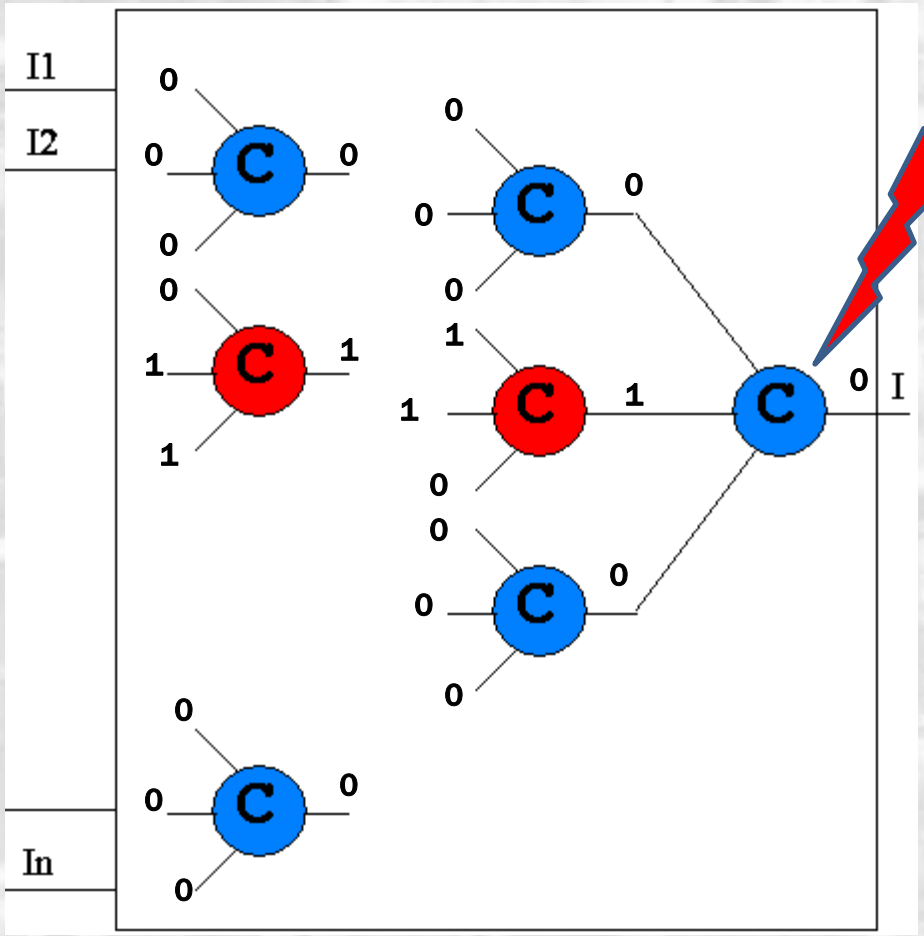
ST register bit's tolerance: 56% → 91%

Indication Subcircuit

First cascade **Tree of C-elements**



Indication Subcircuit

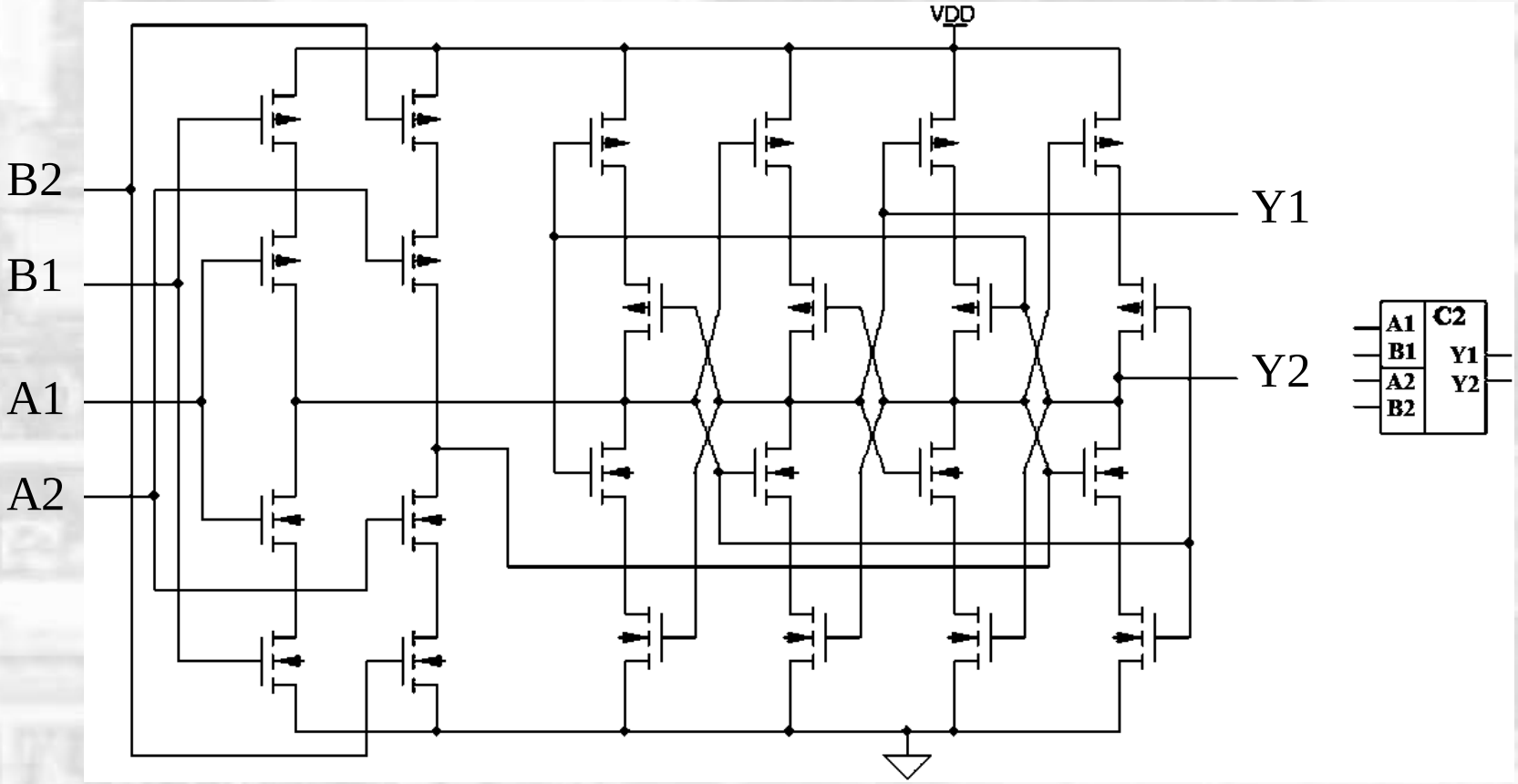


Soft error caused premature C-element's switching

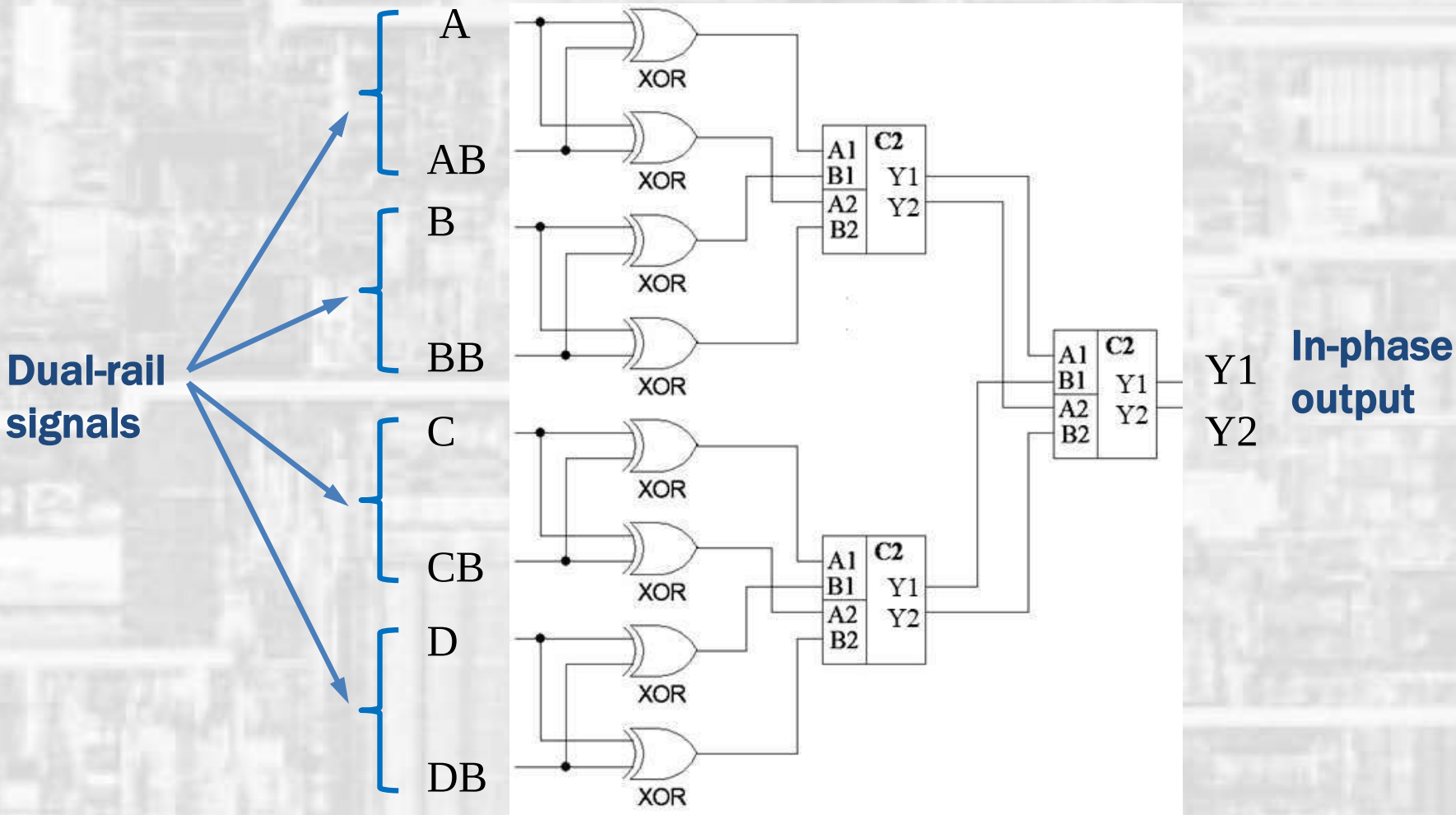
C-element's table

A	B	C	Y^+
0	0	0	0
1	1	1	1
Others			Y

In-Phase C-element



Soft Error Tolerant Indication Subcircuit

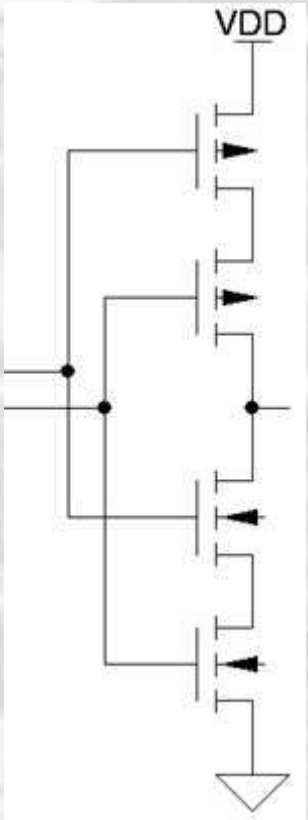


In-phase to Unary Converter

In-phase signals

Y1

Y2



Unary signal

Total Pipeline Tolerance

Self-timed pipeline's stage

Combinational Part	Register	Indication subcircuit
S_{CP}	S_R	S_{IS}

$$S_R \approx S_{IS} \approx 0.5 \cdot S_{CP} \Rightarrow SET = 96\%$$

Conclusions

- One additional transistor in the C-element circuit and cross-links between C-elements prevent "sticking“ register bit in the anti-spacer state
- DICE-like C-element is entirely immune to a single soft error in its internal nodes
- Proposed circuitry and layout techniques, and using in-phase inputs and outputs in the DICE-like C-element improve self-timed pipeline's overall tolerance to single soft errors to a level of not less than 96%

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