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Self-Aligned SHF Structures with Direct and Inverted Ultrathin Emitter Regions

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Abstract—The optimization of the construction and technology of bipolar self-aligned SHF transistor structures with direct and inverted ultrathin emitter regions is carried out. The threshold amplification frequency and maximum oscillation frequency, which are 500 GHz, are shown to be reachable when using self-adjoined pseudo-lithographic masks and decreasing parasitic capacities and resistances. Methods for creating direct and inverted extremely narrow emitter regions doped with arsenic are proposed.

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1. INTRODUCTION

Nowadays, the problem of creating aligned structures on silicon with direct and inverted emitter regions doped with arsenic is topical due to the demand for SHF ICs with operating frequencies of 10–100 GHz and active phased antenna arrays on the crystal surface. In the case of overlying collector regions, a considerable decrease in the base–collector capacities C_{BC} is reached and new possibilities of creating such regions with a small defect density and high breakdown voltage have arisen. The great extent of the regions of structures results in the excessive storage of minority carriers, which decreases the threshold amplification frequency f_t and maximum oscillation frequency f_{max}. This problem is partially solved by developing methods for the exact localization of structures. The development of thin and ultrathin direct and inverted transistor structures on silicon is carried out using the domestic epiplanar technology of lateral dielectric insulation (LDI) with the selective epitaxial growth of Si(As) [1] and arsenic doping in vacuum followed by hydrogen annealing [2–4]. Three-dimensional self-forming transistor structures with flat and narrow emitter regions and selectively deposited tungsten contacts are a special case [5–8]. Interest in the three-dimensional self-forming transistor structures with nanosized elements has increased in recent years [9, 10]. In [11], SHF transistor structures with overlying collector regions and flat inverted emitter regions earthed from below by the continuous layer of metal silicide are studied. These structures are created on SOI silicon plates using ultrathin ($w_{a.b} = 10$ nm) layers of the active base (SiGe:B:C) and have $f_t \approx 95$ GHz and $f_{max} \approx 210$ GHz at the thickness of the silicon layer for the active emitter region of 250 nm, width of emitter windows $w_{e.w} = 500$ nm, and length $L_{e.r} = 1$ μm. The emitter regions are surrounded by the layer of thermal SiO_2 ($h_{EB} = 100$ nm), which is the lateral dielectric insulation of emitter (LDIE) junctions, and the layer of polysilicon Si*(B) doped with boron. These layers can generate residual mechanical stresses σ to emitter regions.

2. CONSTRUCTIONAL FEATURES OF SHF STRUCTURES

In this work, unit SHF self-aligned transistor structures (SATSs) with the emitter region length $L_{e.rl} = 1$ μm and minimum width of emitter windows $w_{e.wl} = 50$ nm, which are completely self-forming in the volume of thin silicon plates without using a typical buried layer, are considered. For $h_{EB} = 50$ nm and width of contacts to base $h_{BC} = 100$ nm, SATSs have the area of the emitter window $A_{e.wl} = 0.05$ μm^2 and area of the collector–base window $A_{CBl} = 0.455$ μm^2. The thicknesses of the lightly-doped (10^{18} atom cm^{-3}) emitter and collector regions adjacent to active regions of the base are $W_e = 10$ nm and $W_C = 20$ nm, respectively. The elementary SATSs are designed to reach the following parameter values: $f_t = f_{max} = 500$ GHz ($r_{Bl}C_{BCl} = 79.8$ Ohm fF; the effective resistance of the base $r_{Bl} = 43.85$ Ohm; the internal resistance of the base $r_{Bi} = 25$ Ohm for $w_{a.b} = 10$ nm and $\rho_{s\,a.b} = 6000$ Ohm/□; and the capacity $C_{CBl} = 1.82$ fF for $C_{CBi} = 4$ fFμm^{-2}). The direct and inverted emitter regions are created based on layers doped with arsenic with the hydrogen annealing. The selectively-deposited tungsten electrodes (with titan sublayer) have the contact resistance $\rho_{CE} \leq 2$ Ohm μm^2. The effective resistance of the emitter regions is determined by the surface resistance of diffused layers ρ_s, as well as the resultant area of emitter A_E, and is critically sensitive to the density and type of structural defects, thickness of the residual matrix

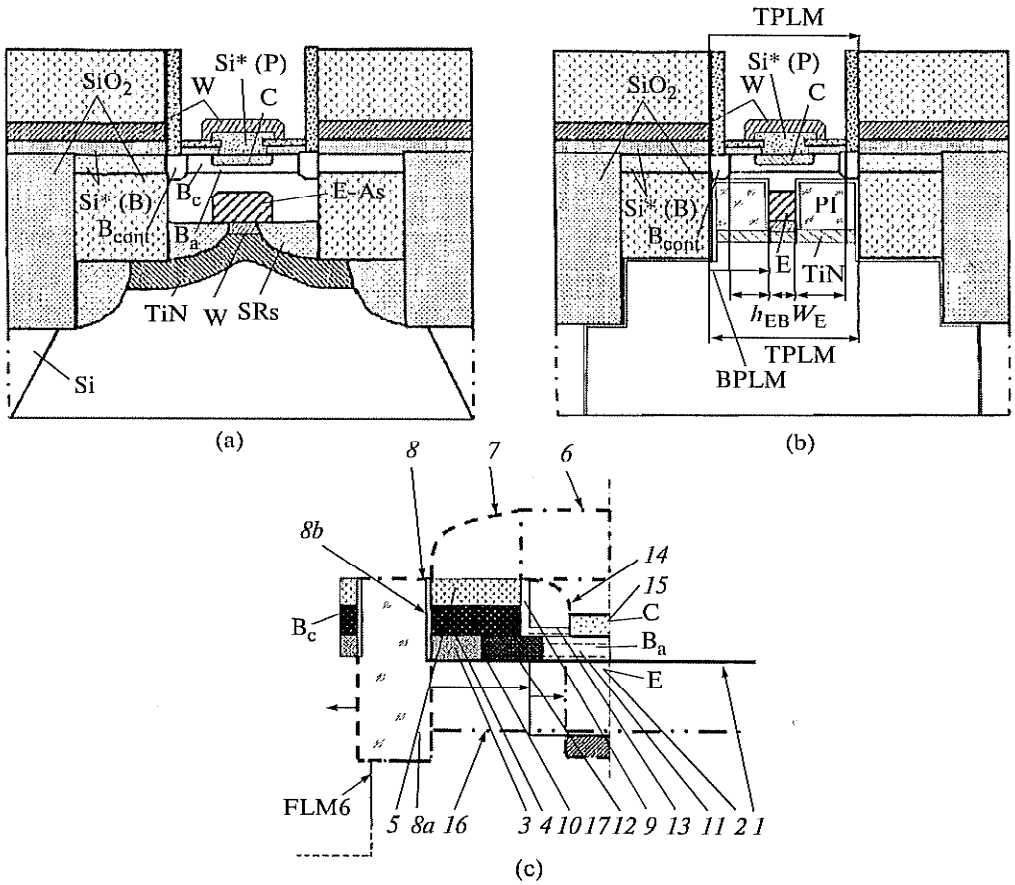

Fig. 1. Constructions of SATSs with inverted emitter regions: (a) with extended diffused emitter region and parasitic butt sections; (b) with narrow self-aligned emitter region and combined LDIE regions based on thin layers of thermal $SiO_2 - SiN_x$ (Al_2O_3, AlN) and polyimidazole film; and (c) with narrow emitter region and selective composite base regions.

oxide, and parameter ρ_{CE}. In order to create exactly localized critical collector and emitter regions, the self-adjunction of the top and bottom pseudo-lithographic masks (TPLMs and BPLMs) with the successive transformation of structure layers (with respect to the initial upper support contour and self-forming relief), which provides the optimal configuration and parameters of the critical regions, is used. Such SATSs must have specific doping profiles with the maximum allowed steep gradients of the ionized concentration [As^+], which are characterized by minimum ρ_s and minimum level of structural defects. These requirements are fulfilled when using special methods of the controlled diffusion of arsenic in vacuum with the homogeneous diffusant source obtained by gas-transport reactions using initial ultrapure materials (Si, As, and J_2) [2, 3, 4]. The constructions of unit SATSs with $L_{c.rl} = 1$ μm are shown in Fig. 1.

The local regions of the collector are made of polysilicone Si* doped with phosphorus; the contact inactive regions of the base (B_{cont}), connective regions of the base (B_c), and active regions of the base (B_a) are exactly localized by using the temporary initial top pseudo-lithographic Si_3N_4 mask 150 nm in thickness [10] (see Fig. 1b). The selective trench etching is performed from the reverse side of the silicon plates up to the bottom parts of LDI regions and emitter–arsenic regions. The inverted emitter regions are created by using spacer regions (SRs) of pyrolytic SiO_2, Si_3N_4, or polysilicon. The exactly localized SRs form the framework for creating BPLM (50–100 nm in thickness) of photoresist or selectively deposited barrier metal (W, Ni). After the etch removal of SRs, the self-aligned mask allows the width of the emitter regions to be reduced by means of anisotropic reactive ion etching (ARIE) and/or chemical etching. Thus, the coupling and exact localization of TPLM and BPLM is reached. This provides the creation of three-dimensional SATSs with channels for the local forced cooling of active regions. The decrease of the SATS' thermal resistance is reached by the partial elimination of polyimide and small LDI regions around the lateral segments of the emitter, as well as by the enlargement

of the TiN metal regions. Superconducting layers can be used in the channels. In the simplest case, the channel regions are filled with an electrochemically deposited layer of gold or copper.

Figure 1c shows the constructional variant of SATS using various pseudo-lithographic masks, together with the uncritical photolithographic mask (FLM) and the selective epitaxy of the base and collector regions. The emitter width can be reduced both from the top through vertical slits and from the reverse side of the silicon plate.

Let us give the sequence of the process of transferring the TPLM image.

1. On the initial surface (*1*) of thin *p*-Si plates, a thin emitter layer (*2*) is formed by the diffusion of arsenic in vacuum and structural layers (*3*) of thermal SiO_2 40 nm in thickness, layer (*4*) of Si*(B) 100 nm in thickness, and layer (*5*) of pyrolytic SiO_2 150 nm in thickness are deposited for the further creation of local regions of the base.

2. Using the technology described in [10], the temporary support layer of pyrolytic SiO_2 (not shown) with vertical walls and spacer Si_3N_4 layer (*6*) with vertical walls for creating the initial PLM1, with composite regions (*7*) of PLM2 with the bottom sublayer of metal (now shown) and temporary protective spacer Si* layer (*7*) being self-formed on its walls, are created.

3. ARIE of trenches (*8*) is performed and the trenches are filled with germanium-silicate glass (*8a*).

4. After the selective elimination of PLM1, layers (*5*) and (*4*) are etched into up to film (*3*) using ARIE, vertical regions (*9*) (Si_3N_4) are self-formed, horizontal slits in layer (*3*) are selectively etched into up to layer (*10*), and composite base regions (*11*) are selectively epitaxially grown based on (*n*-Si) – (SiGe:B:C) – (*n*-Si).

5. During the rapid annealing of SATS, connective regions (*12*) of the p^+-base are self-formed from Si*(B) layer (*4*) by the diffusion of boron.

6. In order to create the collector regions, the passivation layer of thermal SiO_2, masking layer (*13*) of Si_3N_4, and PLM3 based on spacer Si* layer (*14*) are formed and the collector windows are opened.

7. Collector regions (*15*) are self-formed using the selective epitaxy.

8. Using FLM, cavities (*16*) are etched into silicon from the reverse side of SATS using ARIE and are masked with the Si_3N_4 film.

9. Regions (*15*) are protected with photoresist, glass (*8a*) is partially etched out, and vertical PLM4 is formed based on Si_3N_4 film (*8b*) to protect the butt segments of base regions (*3–5*).

10. Glass (*8a*) is etched out, the horizontal regions of the emitter are thinned (shown by arrows), the cavities are filled with glass, and metallization regions (*17*) are formed.

The elementary transistor structures can be connected into parallel sections to form power keys with a different width of emitter regions, which are suspended on metal (or metal-carbon) beams.

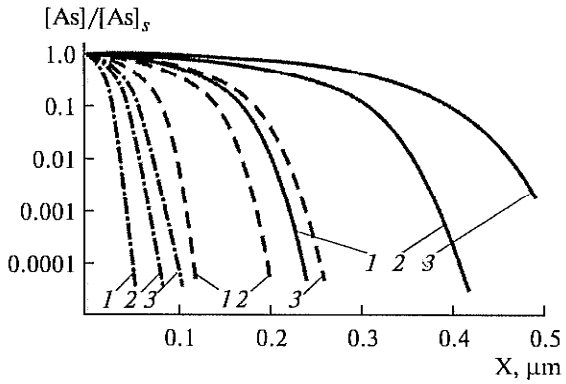

Fig. 2. Calculated distributions of surface-normalized values of the overall concentration of arsenic [As]/[As]$_s$ with respect to the depth of diffused layers for different diffusion time and temperature: *1* is 12 min; *2* is 36 min; *3* is 60 min; —·—·— is 900°C, $D_i = 5.39 \times 10^{-16}$ cm^2/s; – – – is 950°C, $D_i = 2.6 \times 10^{-15}$cm^2/s; and — is 1000°C, $D_i = 1.17 \times 10^{-14}$ cm^2/s.

3. RESULTS OF SIMULATING THE EMITTER REGIONS OF STRUCTURES

The results of solving the boundary problem of calculating the distributions of surface-normalized values of the As's overall concentration are shown in Fig. 2. The refined model of the As diffusion allows for the effect of the internal electric field, changes in the equilibrium concentration of vacancies, complex formation of neutral vacancies with two neutral As atoms [3], and experimental dependencies of $[As^+] = f_1[As]$ and the squared intrinsic concentration of charge carriers $n_i^{*2} = f_2[As^+]$. The minimum thickness of the emitter regions is 50 nm ($\rho_s = 360$ Ohm/□). When creating real SATSs, more thick layers with lower ρ_s can be used with the subsequent thinning using ARIE.

The table gives the calculated and experimental dependences of parameter ρ_s of the diffused layers on the diffusion time *t* for different diffusion temperatures *T*. It can be seen that, for $T = 1000$°C, there is a good agreement between the calculated and the experimental data.

4. FORMATION OF ULTRATHIN TRANSISTOR STRUCTURES WITH A FLAT EMITTER

SATSs are analyzed and optimized with respect to the set of the electrical parameters measured using special benchmark mesa-structures with the internal buried contact to the active regions of the base, with allowance for the detected specific structural defects in the near-surface silicon layer [5]. The defects have a

Calculated and experimental dependencies of ρ_s (Ohm/□) of diffused layers on the diffusion time for different temperatures

Diffusion time, min	Diffusion temperature, °C			
	900	950	1000	1000
	calculation			experiment
10	360	110.75	49.4	50
20	250	82.6	35.4	36
30	200	66.6	27.4	29.5
40	175	57.3	24	25.5
50	150	50.6	21.7	22.3
60	140	46.6	20.0	21.0

strong effect on the leakage currents of ultrathin flat mesa-junctions and parameter ρ_{CE}. In such structures, the coefficient of emitter current transmission h_{21E} is determined by the efficiency of the emitter and depends directly on doping characteristics, leakage currents, and parameter σ in the LDIE regions. For the concentration $[As]_s \approx 10^{21}$ cm^{-3}, the surface erosion takes place. For $[As]_s \approx 8 \times 10^{20}$ cm^{-3}, separate precipitates are observed. For $[As]_s \approx 5 \times 10^{20}$ cm^{-3}, a silicon surface that is almost free from defects can be obtained.

With the decrease in width of the emitter regions, the defects in the emitter region, internal stresses σ, and charge Q, which are introduced by the LDIE regions, have a growing effect on the current-voltage characteristic of the transistor structures. The leakage currents of emitter–base junctions I_{EB} above 10^{-12} A ($U_{EB} \leq 0.4$ V) are observed during the thermal oxidation of the emitter regions. For the SiO_2 thickness of 20 nm and SiN_x thickness of 30 nm, the leakage current I_{EB} depends directly on $[As]_s$ and the density of the structural defects. With the optimal doping and controlled chemical etching of the emitter regions from butt segments, the leakage current I_{EB} is less than 10^{-12} A during the surface passivation of the emitter regions with the thin SiO_{2T} layer in combination with SiN_x (Al_2O_3, AlN) films and the polyimide (PI) layer. When creating trenches for LDIE, the boron-doped regions of the contact base act as an indicator of the end of the process.

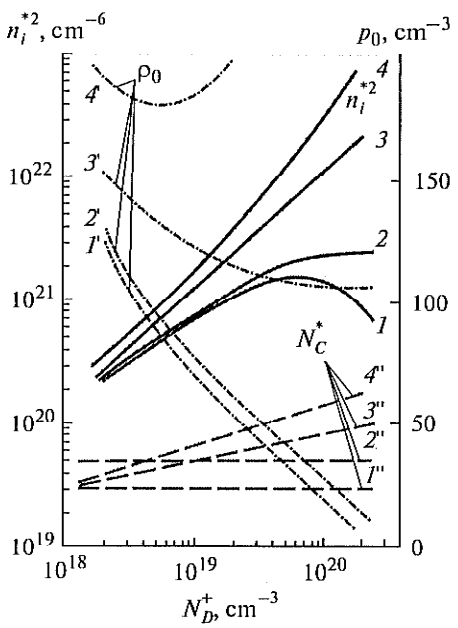

Fig. 3. Calculated dependencies of the physical parameters of the emitter on the doping level: $n_i^{2*}(N_D^+)$ are curves *1–4*; p_0 (N_D^+) are curves *1'–4'*; and $N_C^*(N_D^+)$ are curves *1''–4''*.

Figure 3 shows the calculated dependences of the equilibrium concentration of holes p_0 and the squared intrinsic concentration of charge carriers $n_i^{2*} = p_0 n_0$ as a function of the active concentration of the donor impurity $N_D^+ = [As^+] = n_0$ for different adjustable dependences of the effective density of states $N_C^*(N_D^+)$. For the doping level of the base active region $N_{a.b} \approx 10^{18}$ atom/cm^3, the best agreement between the measured value of the current amplification coefficient h_{21E} of the transistor structure and the calculated value is observed for the dependency of n_i^{2*} (see Fig. 3, curve *3*), which corresponds to the dependency for $N_C^*(N_D^+)$ (see Fig. 3, curve *3''*).

Thus, the possibility in principle of creating completely self-forming SHF transistor structures on thin plates of pure silicon with the calculated values of $f_t = f_{max} = 500$ GHz for direct and inverted narrow and exactly localized flat emitter regions ($L_{e.rl} = 1$ μm, $w_{e.wl} = 50$ nm) with selectively deposited tungsten electrodes is demonstrated. In order to create the collector and emitter regions of the elementary struc-

tures, the self-adjunction of the top and inverted (bottom) pseudo-lithographic masks with the successive transformation of structure layers (with respect to the initial upper support contour and self-forming relief), which provides the optimal configuration and parameters of the critical regions, is used. The elementary transistor structures can be connected into parallel sections to form power keys suspended on metal (or metal-carbon) beams. When creating the ultrathin low-resistance emitter regions doped with arsenic in vacuum, conditions for the origination of specific structural defects, as well as their effect on the current-voltage characteristic of the structures with the flat mesa-emitter, are revealed.

The results can be used to design new methods for the doping and selective growth of materials to create ultrathin self-forming SHF transistor structures. In particular, the formation of the selective collector regions with a high breakdown voltage based on GaP [12] using installations of ultrahigh vacuum and molecular beam epitaxy in vacuum with the gas-phase deposition of layers is promising.

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